NVP6134

Datasheet

4-CH Universal RX(up to 5M RT) and 9-CH Audio Codec

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REVISION HISTORY

Rev.	Date.	Description	Note
REV 0.0	2016-06-08	Initial Draft	-
REV 0.1	2016-08-03	Pin Assignments Modification (XTALI => SYS CLK, XTALO => N.C)	Page 8~10
REV 0.2	2016-08-08	Pin Assignments Modification (N.C PINS => GND PINS, PIN 45 => N.C)	Page 8~10
REV 0.25	2016-10-24	Adding 4M RT format	-
REV 0.3	2016-10-25	Adding 5M RT format	-
			-

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Product Overview

NVP6134 includes Universal 4-Channel RX and 9-Channel Audio Codec. It delivers high quality CVBS, 1M, 2M and 3/4/5M RT image. It accepts separate CVBS, COMET, Universal 1M/2M and 3/4/5M RT inputs from Camera and the other video signal sources. It digitizes and decodes CVBS, COMET, Universal 1M/2M and 3/4/5M RT Analog video signal into digital video components which represents 8-bit BT.656/BT.1120 4:2:2 byte interleave format with 74.25/148.5/297MHz multiplexed.

NVP6134 includes Clock PLL, so each output byte interleave function available. Especially, It is able to use same transmission cable with conventional one for COMET(SD level), 1M/2M(HD/FHD level) and 3/4/5M RT, and they provide the superior-image quality by minimizing the interference when separating Y and C.

9-Channel Audio Codec is 8-Channel Voice/1-Channel Mic PCM Codec which handles voice band signals(300Hz~3400Hz) with 8bit/16bit linear PCM, 8bit G.711(u-law, a-law) PCM. Built-in audio controller can generate digital outputs for recording/mixing and accepts digital input for playback.

4-Channel Universal Coaxial Communication Protocol communicates between controller(DVR) and camera on the video signal through coaxial cable.

Features

1. Video Decoder

- **Input Formats**
  - 4CH Video Input
    : CVBS / COMET
    : Universal 1M/2M and 3/4/5M RT

- **Output Formats**
  - Output in BT.656/BT.1120 4:2:2 byte interleave format with 37.125/74.25/148.5/297MHz
  - Support Sync Separate BT.601 Format (CLK/ H,V-SYNC/ 8'bit DATA)

- **Image Signal Processor**

-. Support Video Standard Auto-Detection up to 5M RT for Each CH
-. Support 4*Video Output Port, Each Port Video Output Format Selectable
-. On Chip Analog CLAMP/Anti-aliasing Filter and EQ Filter
-. Accepts CVBS,COMET, 720P@25p/30p/50p/60p, 1080P@25p/30p, 1536P@25/30p, 1440@25/30p, 1944@20p
-. Robust Sync detection for weak and unstable signals
-. High-performance adaptive comb filter and Notch Filter
-. Programmable H/V Peaking filter for Luminance
-. CTI (Chrominance Transient Improvement)
-. Color compensation for PAL
-. IF compensation filter
-. Robust No-video detection
-. Programmable Brightness, Contrast, Saturation and Hue
-. Programmable Picture Quality Control
-. Programmable Gamma Correction

2. Audio Codec

- 8-Ch Voice / 1-Ch Mic Record, 1-Ch Playback
- 10bit pipe-line ADC / 1*DAC
- In/output Analog PGA Control
- Linear PCM (8bit/16bit, 8K/16K/32K)
- G.711 a-law/u-law (8bits, 8K/16K/32K)
- Input Mixing, Digital Volume, Mute Detection
- SSP/DSP/I2S Interface (Master/Slave mode)
- Cascade mode (up to 2 cascade support)
  : 18-Channel recording (with 2 channel mic recording), mixing output, playback

3. MISC

- Built in Clock PLL
- Single 27M Oscillator for all video standards
- Built in 4-Ch Motion Detector(32x24)
- Support Coaxial Protocols for All Video Standard
- Support Each Channel MPP Pin and IRQ Pin
- Support I2C serial Interface

4. Operating Voltage

- 3.3V/1.2V Supply Voltage

5. Power Consumption

- T.B.D.

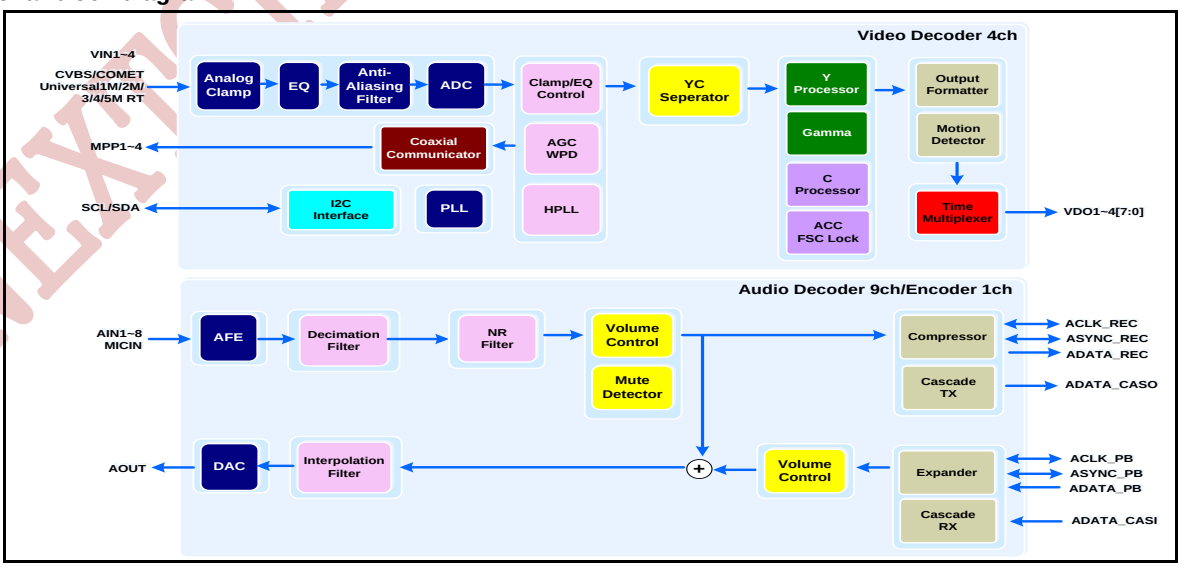
6. Ordering information

DEVICE	PACKAGE	TEMPERATURE RANGE
NVP6134	128e-TQFP	0 ~ 70 ℃

7. Related Products

- HI3520D-V300 / HI3521A / HI3531A

Functional block diagram



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1.1 PIN ASSIGNMENTS

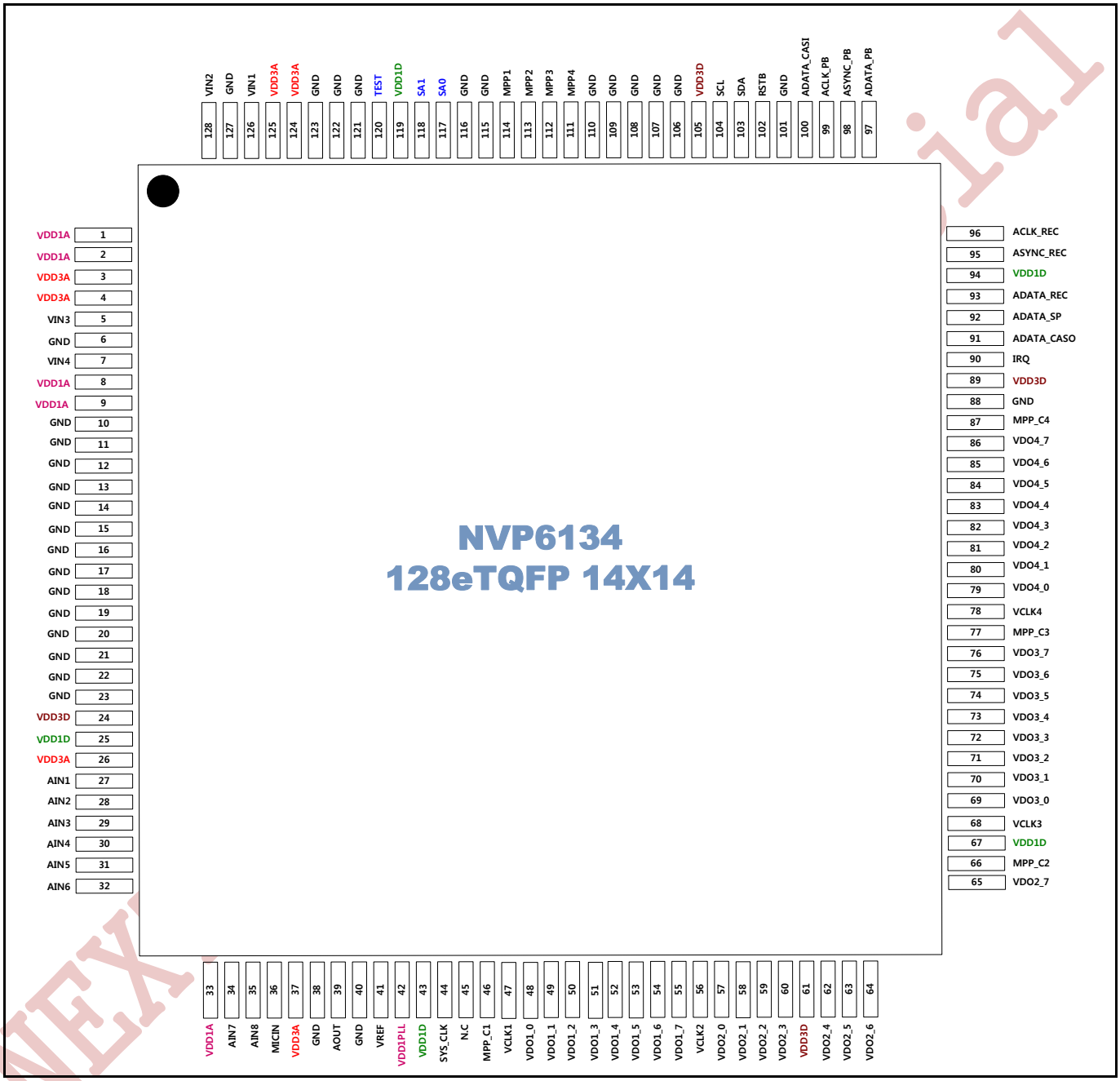


Figure 1.1 Pin Assignments

1.2 PIN DESCRIPTION

Module Name			
NAME	IO	DESCRIPTION	PIN NO.
System Service			
RSTB	DI	System Reset(Active Low)	102
SYS_CLK	DI	Oscillator Input (27MHz)	44
TEST	I	Chip Test mode selection PIN (Normally Connect to Ground)	120
Analog Input Interface			
VIN1	AI	Analog Video Input 1	126
VIN2	AI	Analog Video Input 2	128
VIN3	AI	Analog Video Input 3	5
VIN4	AI	Analog Video Input 4	7
AIN1	AI	Analog Audio Input1	27
AIN2	AI	Analog Audio Input2	28
AIN3	AI	Analog Audio Input3	29
AIN4	AI	Analog Audio Input4	30
AIN5	AI	Analog Audio Input5	31
AIN6	AI	Analog Audio Input6	32
AIN7	AI	Analog Audio Input7	34
AIN8	AI	Analog Audio Input8	35
MICIN	AI	Analog Mic Input	36
ETC			
IRQ	O	Interrupt Request Output	90
ACLK_REC	B	Clock for Record (M:output, S:Input)	96
ASYNC_REC	B	Sync for Record(M:output, S:Input)	95
ADATA_REC	O	Audio Digital Data for Record	93
ADATA_SP	O	Audio Digital Data for Speaker	92
ADATA_CASO	O	Audio Digital Data for Cascade Output	91
ADATA_CASI	I	Audio Digital Data for Cascade Input	100
ACLK_PB	B	Clock for Playback (M:output, S:Input)	99
ASYNC_PB	B	Sync for Playback (M:output, S:Input)	98
ADATA_PB	I	Audio Digital Data for Playback	97
MPP1	O	Coaxial Output1	114
MPP2	O	Coaxial Output2	113
MPP3	O	Coaxial Output3	112
MPP4	O	Coaxial Output4	111
MPP_C1	O	Multi-Purpose Pin Output1	46
MPP_C2	O	Multi-Purpose Pin Output2	66
MPP_C3	O	Multi-Purpose Pin Output3	77
MPP_C4	O	Multi-Purpose Pin Output4	87
DIGITAL Video Interface			
VCLK1	O	Video Output Clock1	47
VDO1[7]	O	Video Data Output 1[7]	55
VDO1[6]	O	Video Data Output 1[6]	54
VDO1[5]	O	Video Data Output 1[5]	53
VDO1[4]	O	Video Data Output 1[4]	52
VDO1[3]	O	Video Data Output 1[3]	51
VDO1[2]	O	Video Data Output 1[2]	50
VDO1[1]	O	Video Data Output 1[1]	49
VDO1[0]	O	Video Data Output 1[0]	48

DIGITAL Video Interface			
VCLK2	O	Video Output Clock2	56
VDO2[7]	O	Video Data Output 2[7]	65
VDO2[6]	O	Video Data Output 2[6]	64
VDO2[5]	O	Video Data Output 2[5]	63
VDO2[4]	O	Video Data Output 2[4]	62
VDO2[3]	O	Video Data Output 2[3]	60
VDO2[2]	O	Video Data Output 2[2]	59
VDO2[1]	O	Video Data Output 2[1]	58
VDO2[0]	O	Video Data Output 2[0]	57
VCLK3	O	Video Output Clock3	68
VDO3[7]	O	Video Data Output 3[7]	76
VDO3[6]	O	Video Data Output 3[6]	75
VDO3[5]	O	Video Data Output 3[5]	74
VDO3[4]	O	Video Data Output 3[4]	73
VDO3[3]	O	Video Data Output 3[3]	72
VDO3[2]	O	Video Data Output 3[2]	71
VDO3[1]	O	Video Data Output 3[1]	70
VDO3[0]	O	Video Data Output 3[0]	69
VCLK4	O	Video Output Clock4	78
VDO4[7]	O	Video Data Output 4[7]	86
VDO4[6]	O	Video Data Output 4[6]	85
VDO4[5]	O	Video Data Output 4[5]	84
VDO4[4]	O	Video Data Output 4[4]	83
VDO4[3]	O	Video Data Output 4[3]	82
VDO4[2]	O	Video Data Output 4[2]	81
VDO4[1]	O	Video Data Output 4[1]	80
VDO4[0]	O	Video Data Output 4[0]	79
AUDIO DAC			
AOUT	AO	Analog Audio Output	39
VREF	AO	Audio DAC Voltage Reference Output	41
I2C Interface			
SCL	I	I2C Interface Clock (3.3V tolerant)	104
SDA	B	I2C Interface R/W Data (3.3V tolerant)	103
SA0	I	Pin1 for Slave Address	117
SA1	I	Pin2 for Slave Address	118
Power			
VDD1PLL	P	PLL Analog Power (1.2V)	42
VDD1D	P	Digital Power (Digital1.2V)	25, 43, 67, 94, 119
VDD3D	P	Digital Power (Digital 3.3V)	24, 61, 89, 105
VDD1A	P	Analog Power (Analog 1.2V)	1, 2, 8, 9, 33
VDD3A	P	Analog Power (Analog 3.3V)	3, 4, 26, 37, 124, 125
No Connect Pin			
NC	NC	Open	45
Ground			
GND	G	Ground	6, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 38, 40, 88, 101, 106, 107, 108, 109, 110, 115, 116, 121, 122, 123, 127
PAD_GND	G	Exposed Pad	129

Table 1.1 NVP6134 PIN Description

Chapter 2
UNIVERSAL RX(1M, 2M and 3/4/5M_RT)

NVP6134 is a 4-Channel Universal RX which delivers high quality images. It accepts separate 4-Channel Universal Inputs from Camera and the other video signal sources.
It digitizes and decodes 4-Channel Universal 1M, 2M and 3/4/5M RT video formats into digital component video which represents 8-bit ITU-R BT.656/1120 4:2:2 format and Sync Separate BT.601 Format with 27/36/37.125MHz, 54/72/74.25MHz and 108/144/148.5/297MHz multiplexed. 54/72/74.25/108/144/148.5/297MHz multiplex function is available, because it is in the range of Clock PLL.

NVP6134 includes 4-Channel analog processing circuit that comprises anti-aliasing filter, ADC, CLAMP and Equalizer filter. It shows the best image quality by adaptive high performance comb filter and vertical peaking filter. It also supports programmable Saturation, Hue, Brightness, Contrast and several function such as CTI, Programmable peaking filter and various compensation filters.

2.1 FUNCTIONAL OVERVIEW

The Universal 1M, 2M and 3/4/5M RT RX separates luminance and chrominance signals from Universal Inputs. Figure 2.1 show the block diagram of the **NVP6134** video processing.

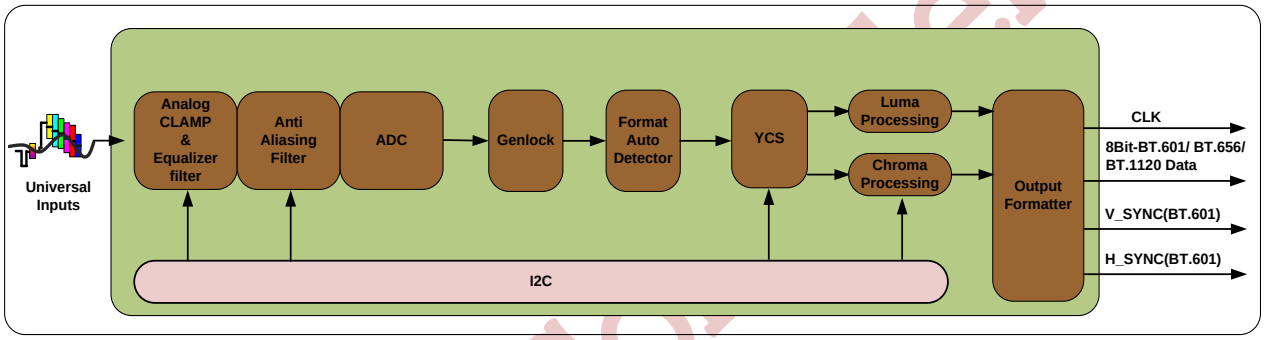


Figure 2.1 Universal RX Video Processing of NVP6134

The First step to decode Universal RX is to digitize the entire video signal using an A/D converter (ADC). Video inputs are usually AC-coupled and have a 75 Ohm AC and DC input impedance. As a result, the video signal must be DC restored every scan line during horizontal sync to position the sync tips at known voltage level using the AGC/CLAMP logic.(AGC)

NVP6134 decides the attenuated image signal level via cable by EQ pattern; compensates the attenuated image signals by equalizer compensation filter. (EQ Pattern)

The video signal also is low-pass filtered in Anti aliasing Filter to remove any high-frequency components that may result in aliasing. Vertical sync and horizontal sync information are recovered in Genlock block.

In regard to various video formats, **NVP6134** has the auto detection module for these video formats which uses different H/V Sync length according to each formats. (Video Standard Auto Detection)

When composite video signal is decoded, the luminance and chrominance are separated by YCS(Y/C Separator).

The quality of decoded image is strongly dependent on the signal quality of separated Y and C. To achieve best quality of image, Adaptive Comb Filter is used.

The color demodulator in chroma processing block accepts modulated chrominance data from Adaptive Comb Filter which generate Cb/Cr color difference data. During active video period, the chrominance data is demodulated using sin and cos subcarrier data.

2.2 VIDEO INPUT FORMATS

NVP6134 supports Universal Video Formats. Table 2.1 show various Video Formats and Register Setting Value (VIDEO_FORMAT, 0x08~0B[4:0], Bank0/ AHD_MD, 0x81~84[3:0], Bank0/ SPL_MD, 0x85~89[3:0], Bank0) to support them.

FORMAT	HZ	H x V	Fsc(MHz)	SPL_MD (Bank0, 0x85~89[3:0])	AHD_MD (Bank0, 0x81~84[3:0])	VIDEO_FORMAT (Bank0, 0x08~0B[4:0])
NTSC-M,J	59.94	720x240 960x240	3.579545	0x0	0x0	0x00
NTSC-4.43	59.94	720x240 960x240	4.43361875			0x11
PAL-B,D,G,H,I	50	720x288 960x288	4.43361875			0x1D
PAL-M	59.94	720x240 960x240	3.57561149			0x16
PAL-Nc	50	720x288 960x288	3.58205625			0x1F
PAL-60	60	720x240 960x240	4.433619			0x15
AHD_5M_20P	20	2592x1944	Flexible	0x5	0x3	Don't care
AHD_4M_30P	30	2560x1440	Flexible	0x0	0xE	
AHD_4M_25P	25	2560x1440	Flexible		0xF	
AHD_3M_30P	30	2048x1536	Flexible	0x4	0x2	
AHD_3M_25P	25	2048x1536	Flexible		0x3	
AHD_1080_30P	30	1920x1080	Flexible	0x0	0x2	
AHD_1080_25P	25	1920x1080	Flexible		0x3	
AHD_720_60P	60	1280x720	Flexible		0x4	
AHD_720_50P	50	1280x720	Flexible		0x5	
AHD_720_30P	30	1280x720	Flexible		0x6	
AHD_720_25P	25	1280x720	Flexible		0x7	

Table 2.1 NVP6134 INPUT VIDEO IMAGE FORMATS

2.3 ANALOG FRONT END (CLAMP, ANTI-ALIASING FILTER, EQ FILTER)

NVP6134 includes 4 Channel Analog Processing circuits that comprise anti-aliasing filter, EQ Filter, ADC and CLAMP. Because its design is dedicated for video application, Analog Processing circuit does not require external reference circuit. External coupling capacitance only is needed for **NVP6134**. Figure 2.2 demonstrates the bode plot of Anti-aliasing Filter. Anti-aliasing Filter is controlled by Register and include bypass mode that don't have AFE filtering.

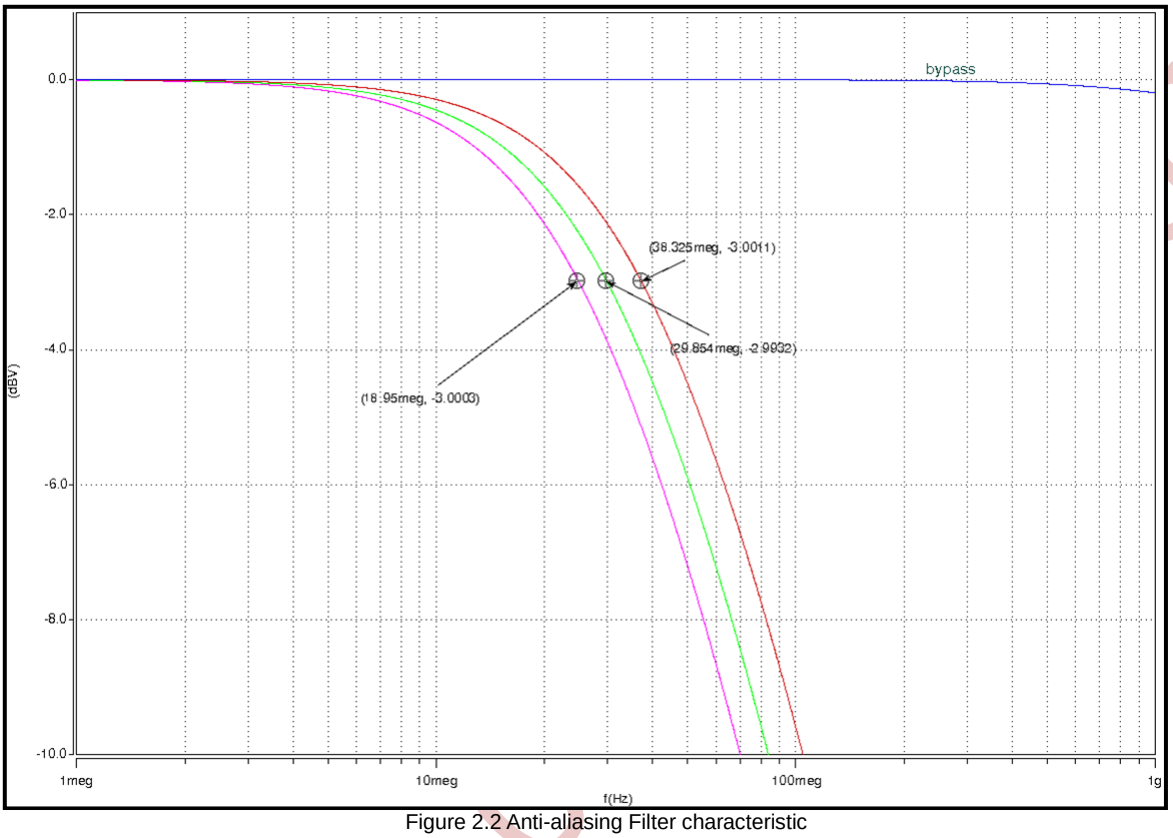


Figure 2.2 Anti-aliasing Filter characteristic

2.4 GENLOCK (ROBUST SYNC DETECTION, ROBUST NO-VIDEO DETECTION)

NVP6134 provides a fully digital Genlocking circuitry. The digital Genlocking Circuitry use the locking method of the timing control signals such as horizontal sync, vertical sync, and the color subcarrier.

NVP6134 uses the proprietary Genlock mechanism for video application system.

It supports very Robust Sync Detection & Robust No-Video Detection, and it is also showed reliable operation in Non-standard signal and Weak-signal.

2.5 YCS (Y/C SEPARATOR)

The YCS is used to separate Y and C signal from Universal HD standard video signal. Therefore, The output image is sharper and clearer compared to other device. To achieve this, BSF(Band Split Filter) is used. Figure 2.3. shows partial Characteristic of BSF. According to Input signal format, BSF characteristic can be selected.

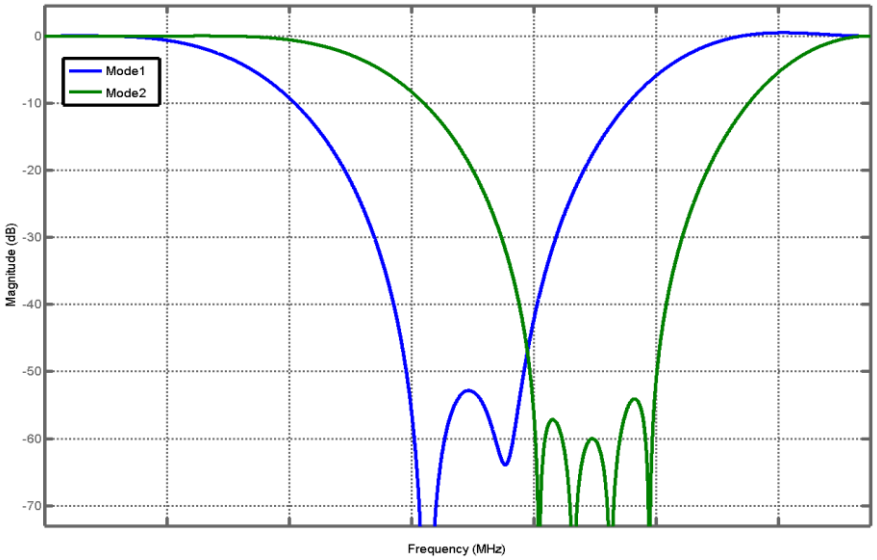


Figure 2.3 Band Split Filter Characteristic

NVP6134 can also separate Y signal from C signal out of input CVBS using the Notch Filter. And according to internal criteria in the **NVP6134**, the Notch and Comb filters can be mixed for use. In special case, use the Notch filter to separate Y signal from C signal to have a good-quality image.

2.6 LUMA PROCESSING

The high-frequency range of Y/C separated data has a relatively smaller magnitude than the low-frequency range. The high-frequency range makes the image more distinct and remarkable, but may induce worse coding efficiencies when video signal is compressed.

Figure 2.4. shows Peaking Filter Characteristic. **NVP6134** provides the peaking filter and Gain control for emphasizing or depressing the high-frequency area to avoid this problem. The Peaking filter is applied to this purpose and its characteristics can be controlled by register (Y_PEAK_MODE, 0x18[7:4] / 0x19[7:4] / 0x1A[7:4] / 0x1B[7:4], Bank0) via I2C interface.

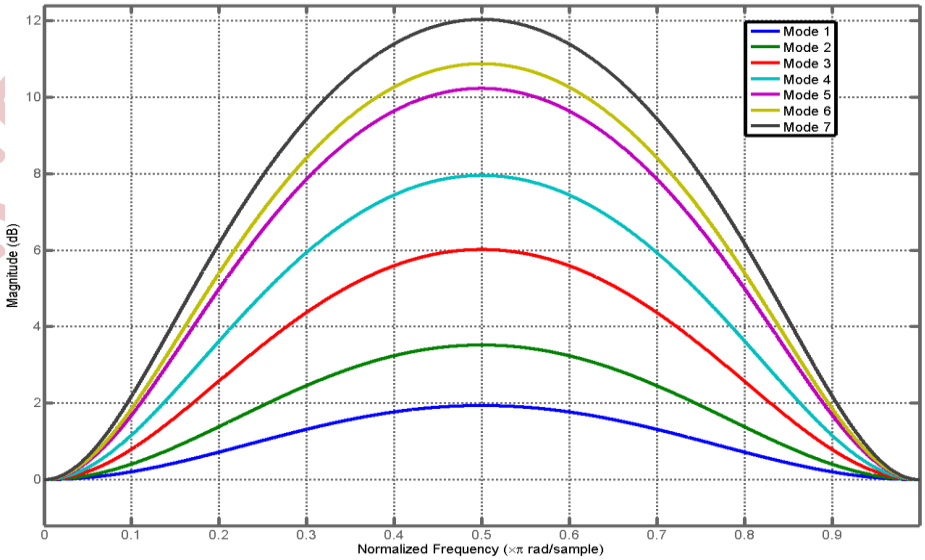


Figure 2.4 Peaking Filter Characteristic

2.7 CHROMA PROCESSING

The Chroma Processing mainly consists of 3 parts: demodulation, filtering, and ACC(Automatic Chroma-gain Control). The Chroma Demodulator receives modulated chroma from YC separator, and generates demodulated color difference data. Demodulated data must be low-pass filtered to reduce anti-aliasing artifacts.

Figure 2.5. shows chroma demodulation and filtering process. Chroma LPF frequency characteristics is demonstrated in Figure 2.6.

Users can select the chroma filter through I2C interface (CLPF_SEL, 0x21/25/29/2D[3:0], Bank0).

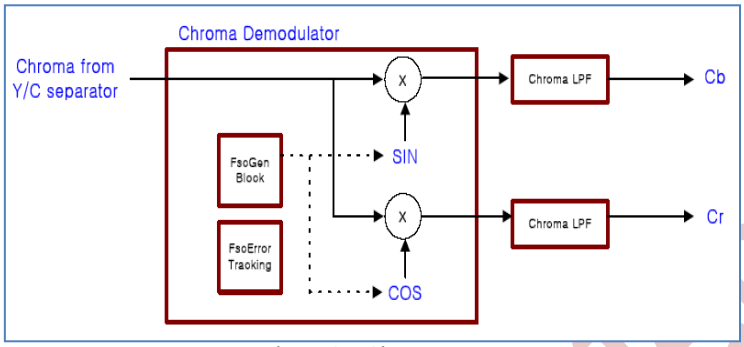


Figure 2.5 Chroma Process

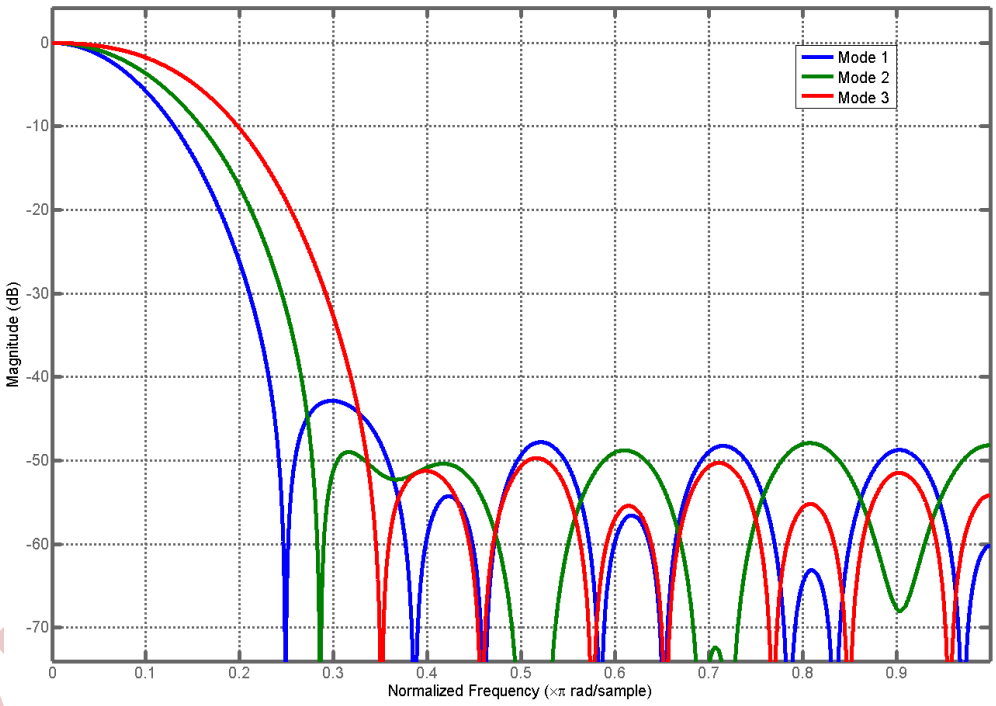


Figure 2.6 Chroma Low Pass filter Characteristic

2.8 DATA OUTPUT ORDER & DIRECTION CONTROL

NVP6134 can change the order of the output pin in the All Output Mode as shown in Table 2.2. (OUT_DATA_x_INV, 0xCB[3:0] Bank1) Furthermore, as Clock and Data pins control direction so may it does nothing with interconnected back-end device and how control related control register as shown in Table 2.3. (VCLK_x_EN, 0xCA[7:4] Bank1 / VDO_x_EN, 0xCA[3:0] Bank1)

Address (Bank1)	*state*	Data Output of Port X
0xCB[0], OUT_DATA_1_INV	0	VDO_1 [7:0]
	1	VDO_1 [0:7]
0xCB[1], OUT_DATA_2_INV	0	VDO_2 [7:0]
	1	VDO_2 [0:7]
0xCB[2], OUT_DATA_3_INV	0	VDO_3 [7:0]
	1	VDO_3 [0:7]
0xCB[3], OUT_DATA_4_INV	0	VDO_4 [7:0]
	1	VDO_4 [0:7]

Table 2.2 Data Output Pin Order Control

Address (Bank1)	*state*	Data Output of Port X
0xCA[4], VCLK_1_EN	0	HI-Z
	1	Output VCLK_1 Enable
0xCA[5], VCLK_2_EN	0	HI-Z
	1	Output VCLK_2 Enable
0xCA[6], VCLK_3_EN	0	HI-Z
	1	Output VCLK_3 Enable
0xCA[7], VCLK_4_EN	0	HI-Z
	1	Output VCLK_4 Enable
0xCA[0], VDO_1_EN	0	HI-Z
	1	Output DATA1 Enable
0xCA[1], VDO_2_EN	0	HI-Z
	1	Output DATA2 Enable
0xCA[2], VDO_3_EN	0	HI-Z
	1	Output DATA3 Enable
0xCA[3], VDO_4_EN	0	HI-Z
	1	Output DATA4 Enable

Table 2.3 Output Clock and Data Direction Control

2.9 OUTPUT FORMAT

NVP6134 supports a format of standard ITU-R BT.656/1120. Ports of 4 is synchronized by each output clock(VCLK_A~VCLK_D). Phase of clock is controlled by VCLK_SEL(BANK1, 0xCC[7:4]~0xCF[7:4]) and VCLK_DLY_SEL(BANK1, 0xCC[3:0]~0xCF[3:0]).

2.9.1 ITU-R BT.656/BT.1120 FORMAT

Codes of SAV and EAV are injected into data stream of ITU-R BT.656/1120 to indicate a start and a end of active. Note that a number of pixel for 1H active line is always constant regardless of the actual incoming line length. Therefore, variance of analog input signal is applied to a blank section except codes of EAV and SAV. Figure 2.7 shows data stream of ITU-R BT.656/1120 format. If length of 1H of analog input signal increase or decrease, number of pixel of 'A' increase or decrease.

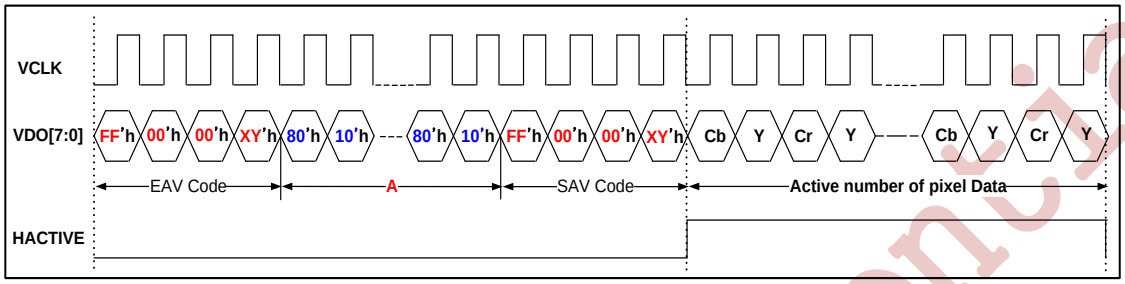


Figure 2.7 Region of active is constant

2.9.2 ITU-R BT.601 FORMAT

NVP6134 support a standard format of ITU-R BT.601.

BT.601 Interface consist of 4 component, 8bit-Video Data, Video Clock, H-SYNC and V-Sync(Figure2.8). NVP6134 can output H/V-SYNC through MPP1~4 pin and Support up to AHD 1080@25/30P two channels.

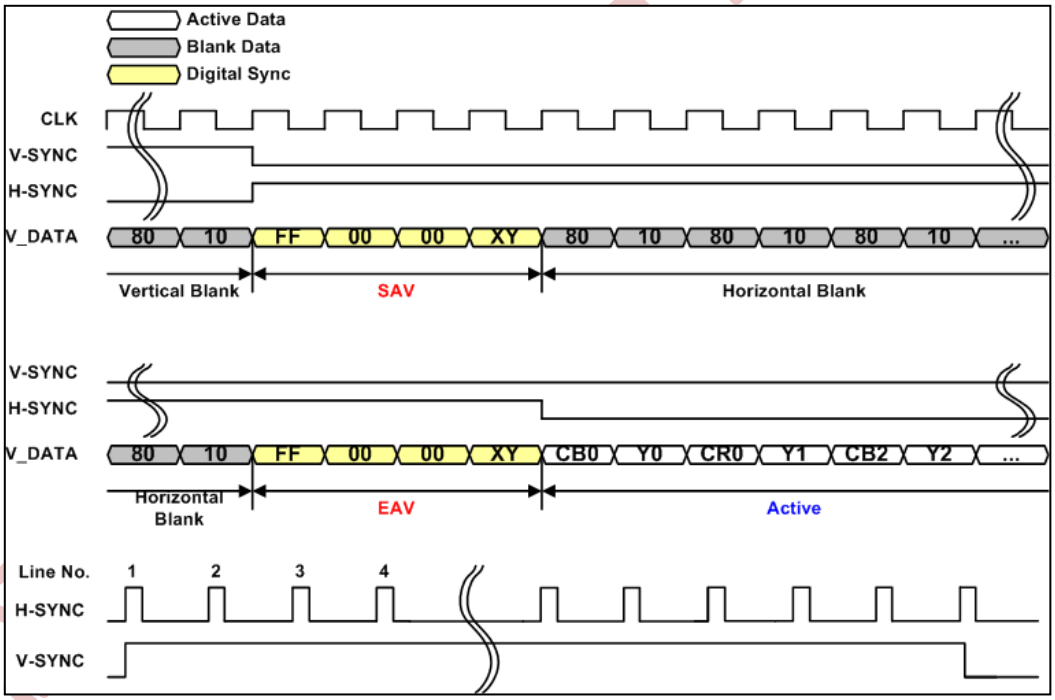


Figure 2.8 BT.601 Interface

2.9.3 VIDEO OUTPUT TIMING INFORMATION

The NVP6134 output timing is like with SD resolution. But some synchronous signals difference with SD resolution as Field information that does not separated EVEN/ODD field. There is next sentence shown timing diagram point of video output.

2.9.3.1 AHD720P @ 30P/25P, 60P/50P H/V Timing

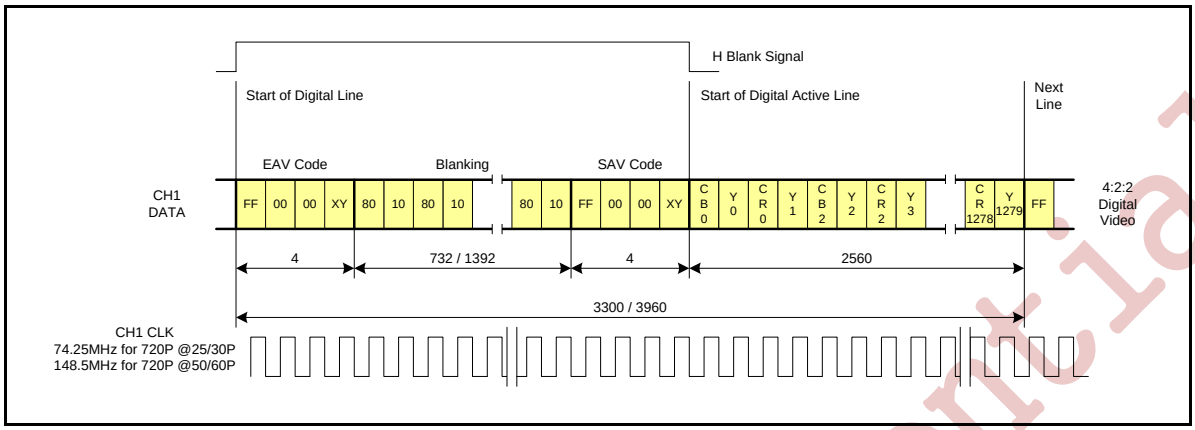
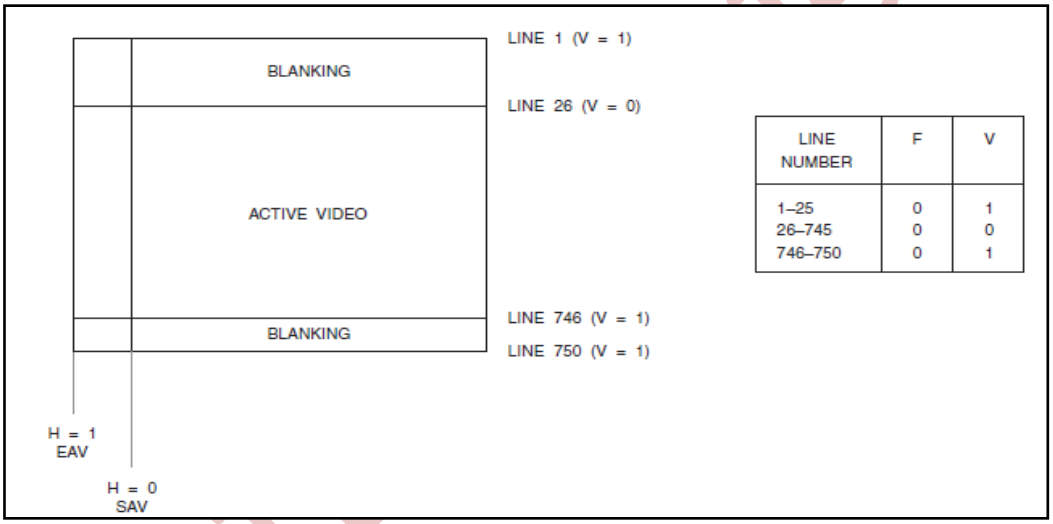


Figure 2.9 AHD720P@30P/25P, 60P/50P Horizontal Timing Diagram



LINE NUMBER	F	V
1–25	0	1
26–745	0	0
746–750	0	1

Figure 2.10 AHD720P@30P/25P, 60P/50P Vertical Timing Diagram

2.9.3.2 AHD1080P @ 30P/25P H/V Timing

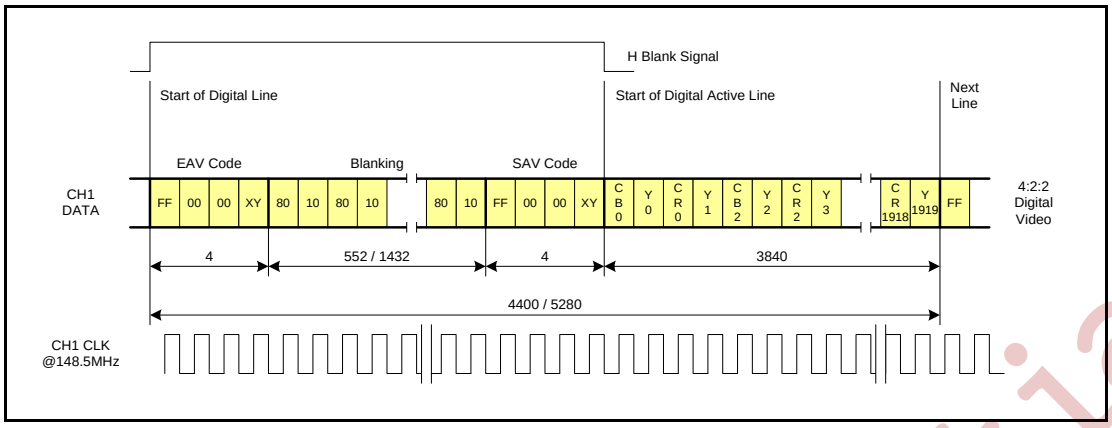
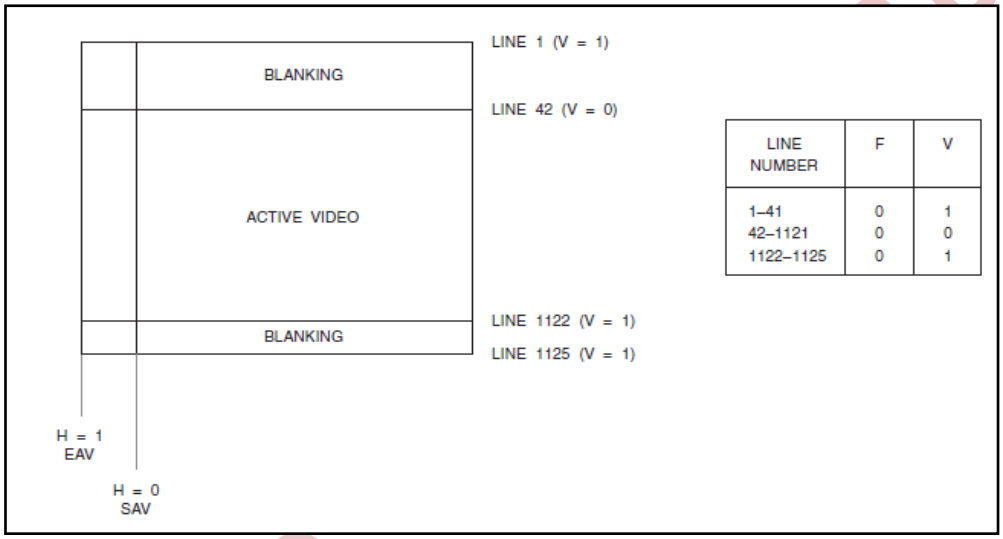


Figure 2.11 AHD1080P@30P/25P Horizontal Timing Diagram



LINE NUMBER	F	V
1–41	0	1
42–1121	0	0
1122–1125	0	1

Figure 2.12 AHD1080P@30P/25P Vertical Timing Diagram

2.10 OUTPUT MODE

The NVP6134 output to the back-end devices whether transferring a channel by a port or 2/4-channels multiplexed output by a port. It is that as much as possible multiplexed channels by a port's output frequency same to sum of multiplexed video's frequency. The NVP6134 supports Variable Output Data Rate.

2.10.1 SINGLE OUTPUT MODE

Codes of SAV and EAV are injected into data stream of ITU-Basically, a video channel output through a port. **NVP6134** output 4-clocks that VCLK1~4 and output 4-data that VDO1~4. There is timing as shown in Figure 2.13. For VCLK1~4 phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Registers(Bank1 0xCC ~CF).

ADDRESS		REGISTER NAME	BITS	VALUE	DESCRIPTION
Bank	Addr				
1	0xC0	VPORT_1_SEQ1	[3:0]	0x0	**VPORT_x_SEQy** **:** Select the type of output video signal through each video output port (x = VDO output port number, y= channel count for 1-port) **0** : Nomal Display of Channel 1 **8** : H_CIF Display of Channel 1 **1** : Nomal Display of Channel 2 **9** : H_CIF Display of Channel 2 **2** : Nomal Display of Channel 3 **A** : H_CIF Display of Channel 3 **3** : Nomal Display of Channel 4 **B** : H_CIF Display of Channel 4 **Etc.:** Don't use
	0xC2	VPORT_2_SEQ1	[3:0]	0x1	
	0xC4	VPORT_3_SEQ1	[3:0]	0x2	
	0xC6	VPORT_4_SEQ1	[3:0]	0x3	
	0xC8	VPORT_1_CH_OUT_SEL	[3:0]	0x00	**VPORT_x_CH_OUT_SEL** **:** Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number) **0** : 1-Port 1CH data **2** : 1-Port 2CH time-mixed data **8** : 1-Port 4CH time-mixed data **Etc.:** Don't use
		VPORT_2_CH_OUT_SEL	[7:4]		
	0xC9	VPORT_3_CH_OUT_SEL	[3:0]	0x00	
		VPORT_4_CH_OUT_SEL	[7:4]		

Table 2.4 1Port 1-Channel Normal mode or X-Format Setting

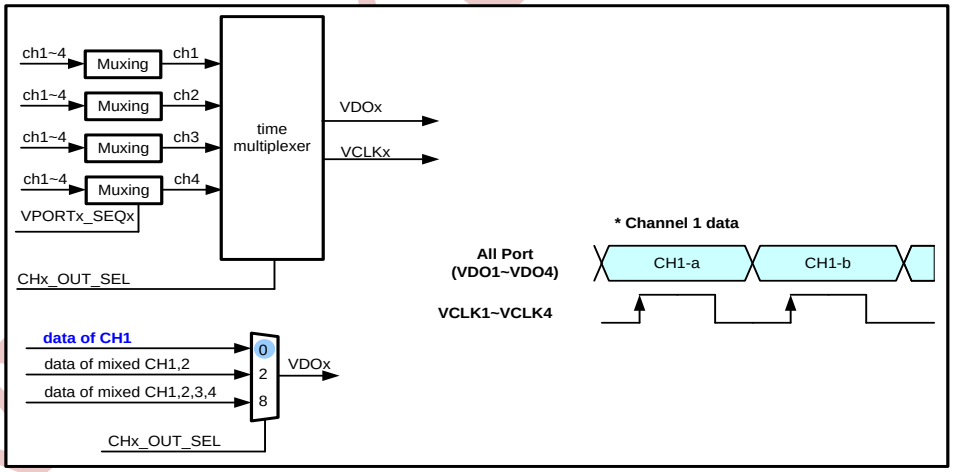


Figure 2.13 Block Diagram of Single-Channel Output

2.10.2 2-MULTIPLEX OUTPUT MODE

In the 2-Multiplex Output Mode, NVP6134 outputs multiplexed 2-channels video through one port. Also, NVP6134 supports the 1Port 2-Channel X-Format Mode. X-Format lowers the Horizontal Frequency in half.

1Port-2CH Normal or Horizontal half mode Setting Value is as below.(Table2.5)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			Normal MODE	X_ MODE	
1	0xC0	VPORT_1_SEQ1	[3:0]	0x10	0x98	**VPORT_x_SEQy** **:** Select the type of output video signal through each video output port (x = VDO output port number, y= channel count for 1-port) **0** : Nomal Display of Channel 1 **8** : H_CIF Display of Channel 1 **1** : Nomal Display of Channel 2 **9** : H_CIF Display of Channel 2 **2** : Nomal Display of Channel 3 **A** : H_CIF Display of Channel 3 **3** : Nomal Display of Channel 4 **B** : H_CIF Display of Channel 4 **Etc.:** Don't use
		VPORT_1_SEQ2	[7:4]			
	0xC2	VPORT_2_SEQ1	[3:0]	0x32	0xBA	
		VPORT_2_SEQ2	[7:4]			
	0xC4	VPORT_3_SEQ1	[3:0]	0x10	0x98	
		VPORT_3_SEQ2	[7:4]			
	0xC6	VPORT_4_SEQ1	[3:0]	0x32	0xBA	
		VPORT_4_SEQ2	[7:4]			
	0xC8	VPORT_1_CH_OUT_SEL	[3:0]	0x22		**VPORT_x_CH_OUT_SEL** **:** Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number) **0** : 1-Port 1CH data **2** : 1-Port 2CH time-mixed data **8** : 1-Port 4CH time-mixed data **Etc.:** Don't use
		VPORT_2_CH_OUT_SEL	[7:4]			
	0xC9	VPORT_3_CH_OUT_SEL	[3:0]	0x22		
		VPORT_4_CH_OUT_SEL	[7:4]			

Table 2.5 1Port 2-Channel Normal mode or X-Format Setting

Figure2.14 shown as multiplexed with 2-channels video output to VDO1~VDO4. For VCLK1~VCLK4 phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register(Bank1 0xCC ~ CF).

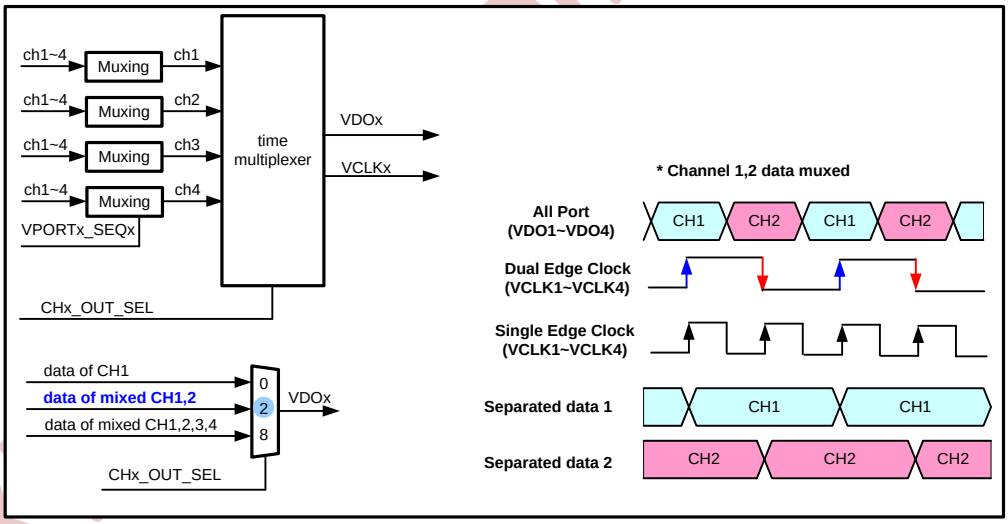


Figure 2.14 Block Diagram of of Multiplexed 2-Channels Output

2.10.3 4-MULTIPLEX OUTPUT MODE

In the 4-Multiplex Output Mode, NVP6134 output multiplexed 4-channels video through in a port. Also, NVP6134 support the 1Port 4-Channels X-Format Mode. X-Format lowers the Horizontal Frequency in half.

1Port-4CH Normal or Horizontal half mode Setting Value is as below. (Table 2.6)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			Normal MODE	X_ MODE	
1	0xC0	VPORT_1_SEQ1	[3:0]	0x10	0x98	**VPORT_x_SEQy** **:** Select the type of output video signal through each video output port (x = VDO output port number, y= channel count for 1-port) **0** : Nomal Display of Channel 1 **8** : H_CIF Display of Channel 1 **1** : Nomal Display of Channel 2 **9** : H_CIF Display of Channel 2 **2** : Nomal Display of Channel 3 **A** : H_CIF Display of Channel 3 **3** : Nomal Display of Channel 4 **B** : H_CIF Display of Channel 4 **Etc.:** Don't use
		VPORT_1_SEQ2	[7:4]			
	0xC1	VPORT_1_SEQ3	[3:0]	0x32	0xBA	
		VPORT_1_SEQ4	[7:4]			
	0xC2	VPORT_2_SEQ1	[3:0]	0x10	0x98	
		VPORT_2_SEQ2	[7:4]			
	0xC3	VPORT_2_SEQ3	[3:0]	0x32	0xBA	
		VPORT_2_SEQ4	[7:4]			
	0xC4	VPORT_3_SEQ1	[3:0]	0x10	0x98	
		VPORT_3_SEQ2	[7:4]			
	0xC5	VPORT_3_SEQ3	[3:0]	0x32	0xBA	
		VPORT_3_SEQ4	[7:4]			
	0xC6	VPORT_4_SEQ1	[3:0]	0x10	0x98	
		VPORT_4_SEQ2	[7:4]			
	0xC7	VPORT_4_SEQ3	[3:0]	0x32	0xBA	
		VPORT_4_SEQ4	[7:4]			
	0xC8	VPORT_1_CH_OUT_SEL	[3:0]	0x88		**VPORT_x_CH_OUT_SEL** **:** Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number) **0** : 1-Port 1CH data **2** : 1-Port 2CH time-mixed data **8** : 1-Port 4CH time-mixed data **Etc.:** Don't use
		VPORT_2_CH_OUT_SEL	[7:4]			
	0xC9	VPORT_3_CH_OUT_SEL	[3:0]	0x88		
		VPORT_4_CH_OUT_SEL	[7:4]			

Table 2.6 1Port 4-Channel Normal mode or X-Format Setting

NVP6134 support the 297MHz 1Port 4CH HD Data Out Mode. Four Channel HD data stream represents 8bit BT.656/1120 4:2:2 format with 297MHz multiplexed. Figure2.15 shown as multiplexed with 4-channels video output to VDO1~VDO4. For VCLK1~VCLK4 phase adjustment can be made against VDO1~VDO4 using "Clock Delay Control" Register(Bank1 0xCC ~ CF).

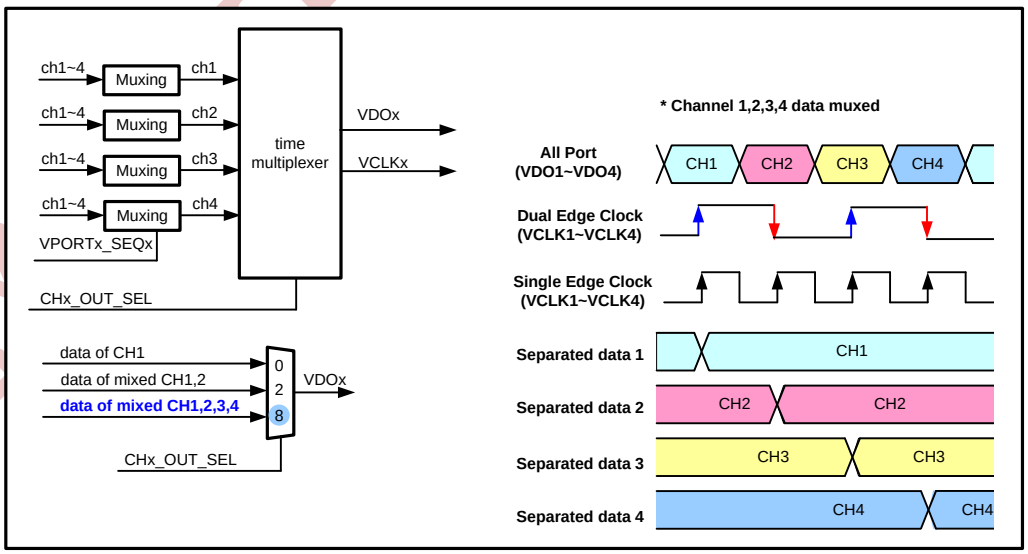


Figure 2.15 Block Diagram of Multiplexed 4-Channels Output

- Example of 297MHz 1Port 4-Channels Data Output Mode with Channel ID

1. In case of VDO1 output port and VCLK1 output clock use.

2. Set VDO1 output(CH_OUT_SEL1, BANK1, 0xC8[3:0] = 0x8) and VCLK1 output (VCLK1_SEL, BANK1,0xCC[7:4] = 0x4 or 0x5) .

3. Set Channel ID Type (Refer to CHID_TYPE(Bank0, 0x54[2:0]) Register Description)

4. And then NVP6134 generate 297MHz(1Port 4CH) data output (Figure 2.16)

If you want to confirm the 297MHz Data using FPGA or Other device, Execute 5~11 item in next page.

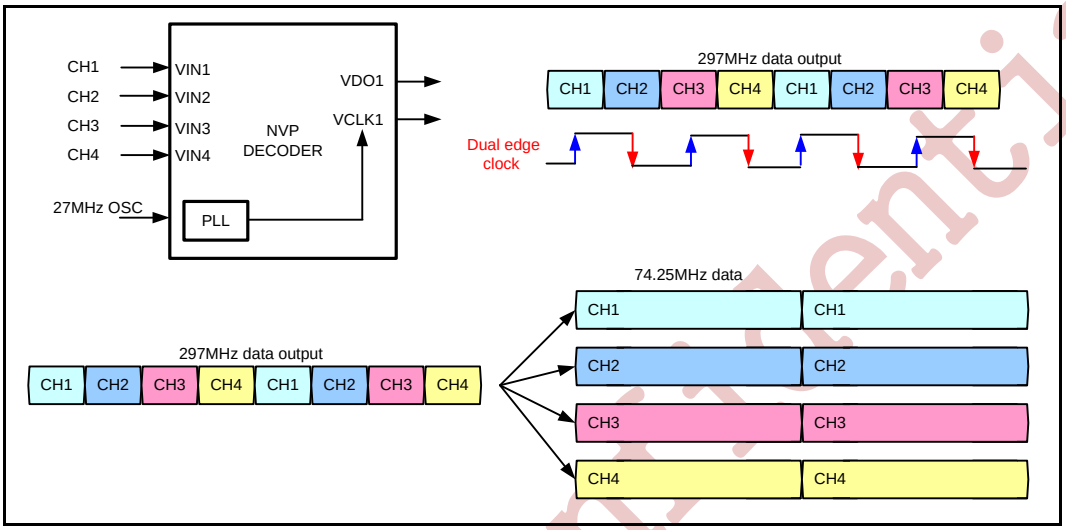


Figure 2.16 NVP6134 generate 297MHz(1Port 4-CH) data output

5. FPGA or equivalent devices which is input 297MHz time multiplexed data output, need to align with same channel data. (74.25MHz 1,2,3,4 channel). Figure2.17. shows how to use Channel ID as a example.

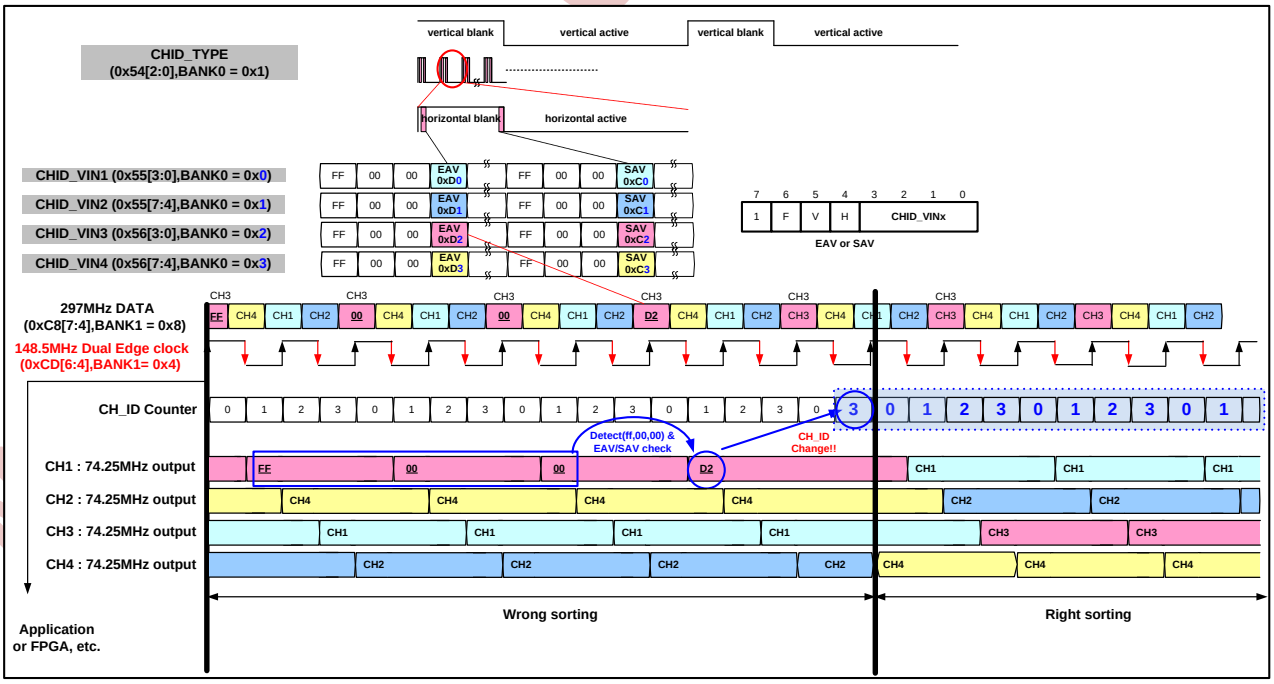


Figure 2.17 NVP6134 Select Channel ID

6. CHID_TYPE(BANK0, 0x54[2:0]=001) mode described in top of Figure2.17.

7. To generate 2bit digit, Design 2bit counter with VCLK1 (The 2bit digit means each channel).

8. Using 2bit digit, Convert from 297MHz Data to 74.25MHz Data (Wrong sorting part in Figure2.17.) and then Define the 2bit digit (0 : Ch1 data, 1 : Ch2 data, 2 : Ch3 data, 3 : Ch4 data).
namely, 297MHz data output separate only with 74.25MHz, 4channel data, is not align with channel data where becomes mapping in counter value.

9. For mapping between separated each channel data and specified counter value, Select channel among separated each channel (1CH selected in Figure2.17.). If selected channel data become Right sorting condition, other 3 channel is sorted automatically.

10. Check the 1ch data output when 2bit counter value is only '0' and then Search the EAV/SAV[3:0] after FF 00 00 Code.

11. If the EAV/SAV[3:0] is '2', make a counter reset to '3' (Refer to Blue color in Figure2.17.)

12. Become Right sorting part.

2.11 297MHz INTERFACE AND MULTI STANDARD OUTPUT MODE

NVP6134 supports the frequency of output data up to 297MHz at maximum. Two Channel FHD data stream represents 8bit BT.656/1120 4:2:2 format with 297MHz multiplexed 1-port. Also, NVP6134 can output 2ch or 4ch signals with different standards(CVBS, 720p, 1080p) through 1-port.

Avaliable output combinations are as below.

(1) 1-port 2-Channel combination

a. CVBS + 720P

b. CVBS + 1080P

c. 720P + 1080P

d. 1080P + 1080P

(2) 1-port 4-Channel combination

a. CVBS 2CH + 720P 2CH

b. CVBS 2CH + 1080P_X 2CH

c. CVBS + 720P + 1080P_X 2CH

d. 720P 4CH

e.1080P_X 4CH

2.12 Video Frame Control

The **NVP6134** supports that a frame control of video output. So it is function that the decoder's output masking by the EAV/SAV make to blank region. If set to FRM_NRT_ON is High, so output finally which set by FRM_NRT_SEQ[29:0] that each a bit of FRM_NRT_SEQ[29:0] match to each a frame. And the FRM_NRT_SEQ rotates continuous then to end from FRM_NRT_SEQ[0] to FRM_NRT_SEQ[29]. If the FRAME_NRT_SEQ bit set to Low, a apply frame has blank region. So, It received back-end device nothing to do because is not active region.

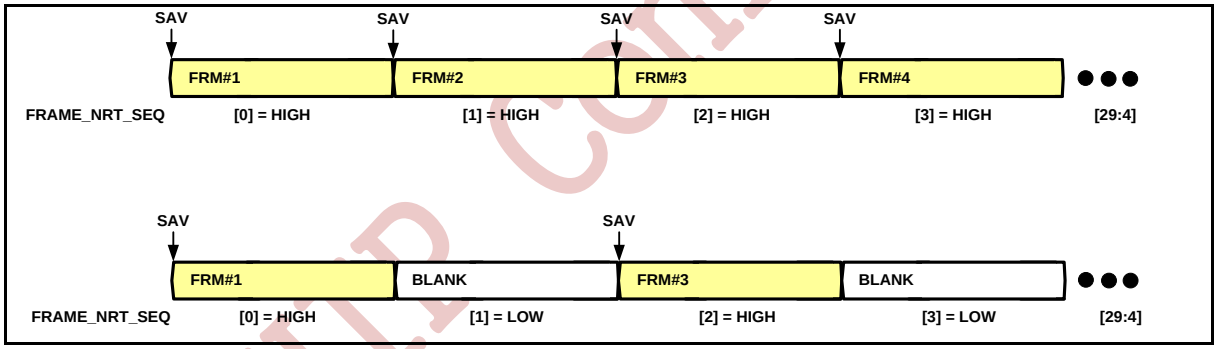


Figure 2.18 Method for Control Video Frame

2.13 MOTION DETECTOR

NVP6134 supports 4-Channels motion detection function. It supports the output of the detected motion information on the screen. The function allows a screen such as the one shown in Figure 2.19. to be divided in 192 sections each of which can generate information on the motion detection information.

For each section, motion detection can be controlled to be set at on/off. Once a motion is detected, the screen can be rendered dark or reversed in the unit of field to have the spot of the motion generated to be indicated in the screen.

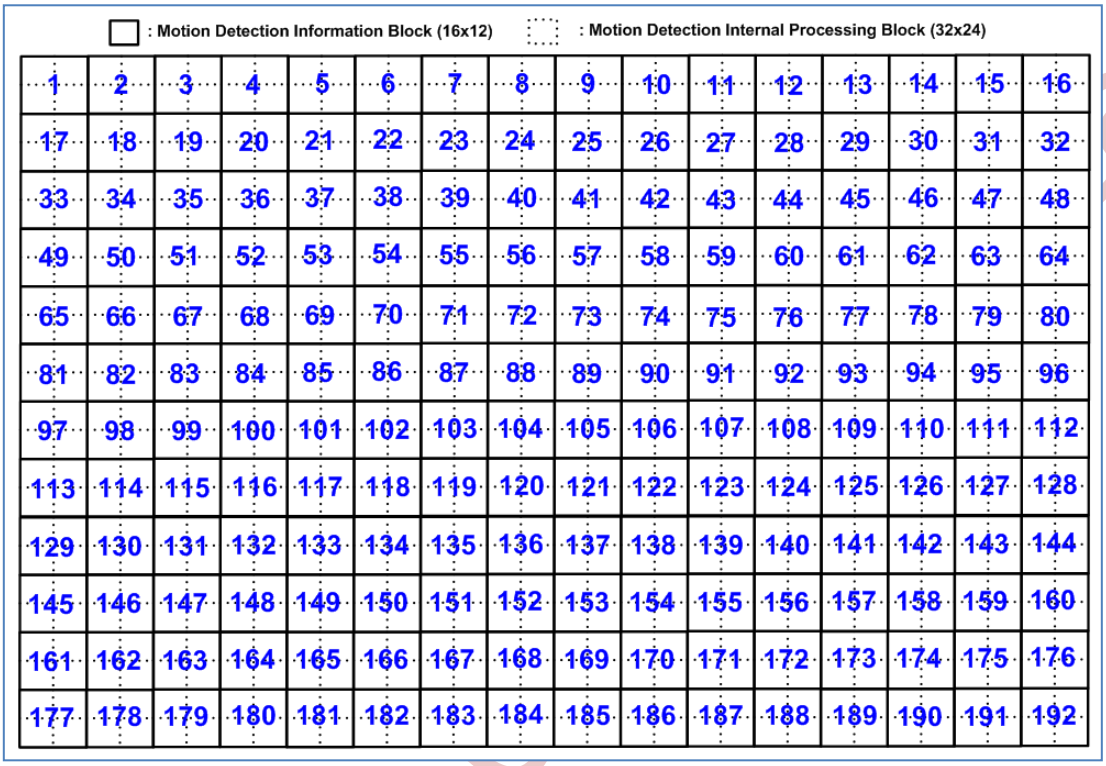


Figure 2.19 Motion Block Mapping

Chapter 3
AUDIO CODEC

NVP6134 outputs PCM digital audio signals converted from analog audio input signals and analog audio signals converted from PCM digital audio signals. **NVP6134** has 9 channels ADC and 1 channel DAC for audio signal.

Audio data convert to G.711 PCM and Linear PCM data, and these converted data is outputted via DSP/SSP/I2S interfaces. The output data will be saved at hard disk or any other storages. This process - to convert and save audio data into storage - is usually called as "Record Output".

The saved audio data is inputted to **NVP6134** via DSP/SSP/I2S interfaces. The input audio data is outputted via audio DAC. This process is named as "Playback Output".

NVP6134 selects one audio input signal among 9 analog audio input(8-Ch Audio/1-Ch mic) and this audio is outputted through audio ADC and audio DAC. And it also supports directly mixed audio output signal which 9 analog audio inputs are mixed. This function usually is called by "Live Output".

In addition, **NVP6134** supports audio mute detection and cascade function up to 2 chips - 18 audio channels(16-Ch Audio/2-Ch mic)

3.1 Record Output

Analog audio data is converted to PCM data and this data is outputted to the other **NVP6134** or other IC via DSP/SSP/I2S interfaces. Record output is useful function to save compressed audio data into storage. Analog audio signal is finally outputted to ADATA_REC pin used for data of each channel and ADATA_SP pin used for one mixed signal of each channel's data. The output data from ADATA_SP pin is either same data of ADATA_REC pin or mixed signal of each channel's data.

PCM data is categorized based on sampling frequency, sampling data bit width and PCM method. G.711 (A-law/Mu-law), unsigned linear PCM and linear PCM are supported. 8KHz / 16KHz and 8bit/16bit are used for sampling frequency and sampling data bit width, respectively. Refer the following table when you set the register value.

	BANK1											
	8K/8bit		8K/16bit		16K/8bit		16K/16bit		32K/8bit		32K/16bit	
	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE	ADDR	VALUE
Linear PCM	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	0 0 1 00	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	0 0 0 00	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	0 1 1 00	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	0 1 0 00	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	1 1 1 00	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	1 1 0 00
Unsigned Linear PCM	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	0 0 1 01	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	0 0 0 01	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	0 1 1 01	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	0 1 0 01	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	1 1 1 01	0x00[0] 0x07[3] 0x07[2] 0x08[5:4]	1 1 0 01
G.711 U-law	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	0 0 1 10 0	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	0 0 0 10 0	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	0 1 1 10 0	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	0 1 0 10 0	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	1 1 1 10 0	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	1 1 0 10 0
G.711 A-law	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	0 0 1 10 1	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	0 0 0 10 1	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	0 1 1 10 1	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	0 1 0 10 1	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	1 1 1 10 1	0x00[0] 0x07[3] 0x07[2] 0x08[5:4] 0x08[6]	1 1 0 10 1

Table 3.1 Sampling & PCM coding setting

DSP / SSP / I2S interfaces are supported as output data format. In addition, slave mode and master mode are also supported. At slave mode, input clock and synchronized signal come from external ICs, however Master mode generates clock and synchronized signal in itself.

3.1.1 Data Output Interface

NVP6134 outputs "Record Output" using ACLK_REC, ASYNC_REC, ADATA_REC and DATA_SP. ACLK_REC is a reference clock signal for Record Output Data and ASYNC_REC is a reference synchronization signal for Record Output Data. ADATA_REC and ADATA_SP are synchronized Record Output, data with reference clock and reference synchronized signal.

	BANK1					
	DSP		SSP		I2S	
	ADDR	*VALUE*	*ADDR*	*VALUE*	*ADDR*	*VALUE*
Master	0x07[0] 0x07[1] 0x07[7]	1 0 1	0x07[0] 0x07[1] 0x07[7]	1 1 1	0x07[0] 0x07[1] 0x07[7]	0 0 1
Slave	0x07[0] 0x07[1] 0x07[7]	1 0 0	0x07[0] 0x07[1] 0x07[7]	1 1 0	0x07[0] 0x07[1] 0x07[7]	0 0 0

Table 3.2 Record Output Interface configuration

ACLK_REC is a reference clock of Record Output Data and ASYNC_REC is reference synchronized signal. ACLK_REC and ASYNC_REC signal support slave mode accepted external signals and master mode generating clock and synchronization signal in itself. And DSP/SSP/I2S interfaces are supported by configuration of these pins defined by internal register setting value.

Figure 3.1, 3.2, 3.3 shows timing diagram of I2S, DSP, and SSP mode, respectively.
These figures show timing relation among ASYNC_REC, ACLK_REC and ADTA_REC, and ADATA_SP is outputted using same interface method of ADATA_REC. Polarity of ACLK_REC clock is changed by setting of internal register value (RM_CLK, 0x07[6], BANK1).

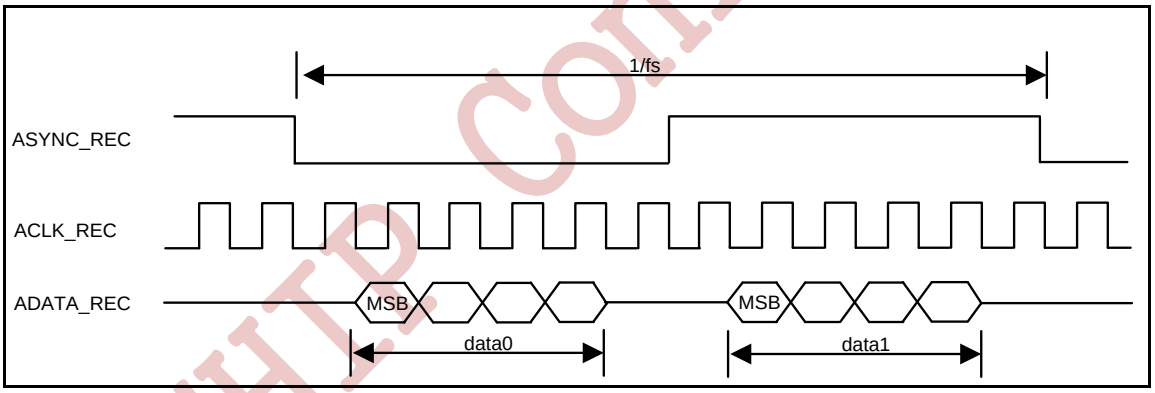


Figure 3.1 Timing of I2S mode

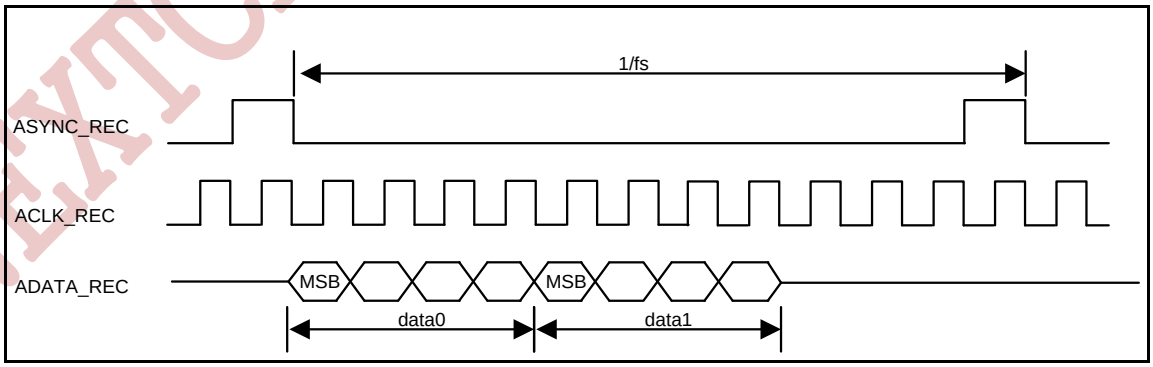


Figure 3.2 Timing of DSP mode

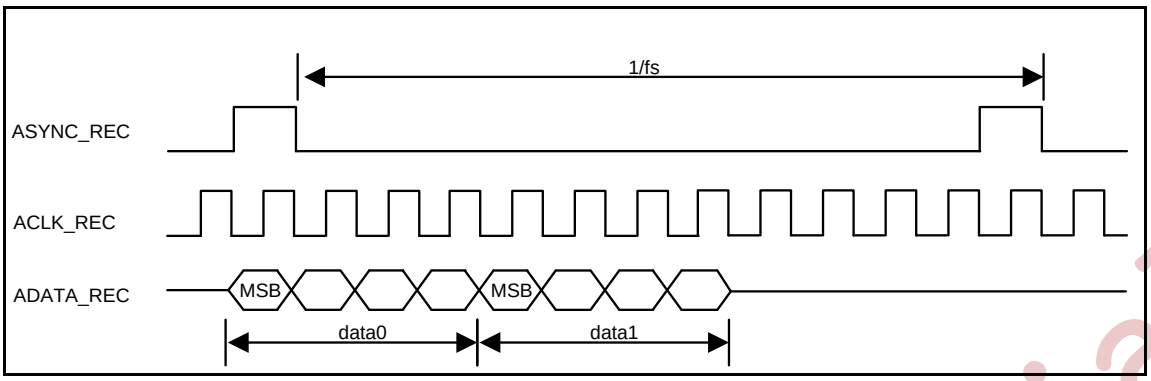


Figure 3.3 Timing of SSP mode

3.1.2 2/4/8/16-Channel Data Output(256 fs)

ADATA_REC supports up to 8 channel audio using single chip and up to 16 channel audio in cascade mode. In this case, the bit-rate of the audio signal should be 256 fs(RM_BITRATE, 0x07[5:4], BANK1). The number of output channel is configured by internal register value (R_MULTCH, 0x08[1:0], BANK1) and the order of output channel is configured by internal register value (R_SEQ, 0x09 ~ 0x12, / MIC_SEQ, 0x3C ~ 0x3D, BANK1).

Therefore, the order of audio output can be changed.

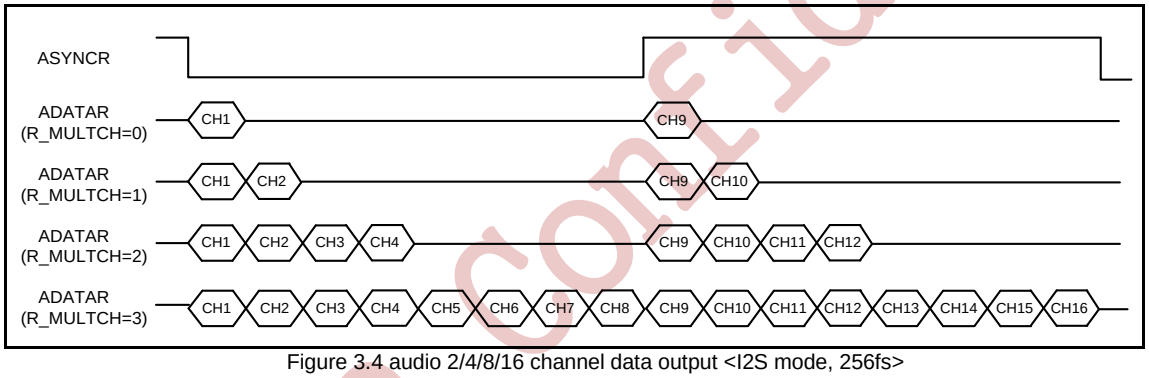


Figure 3.4 audio 2/4/8/16 channel data output <I2S mode, 256fs>

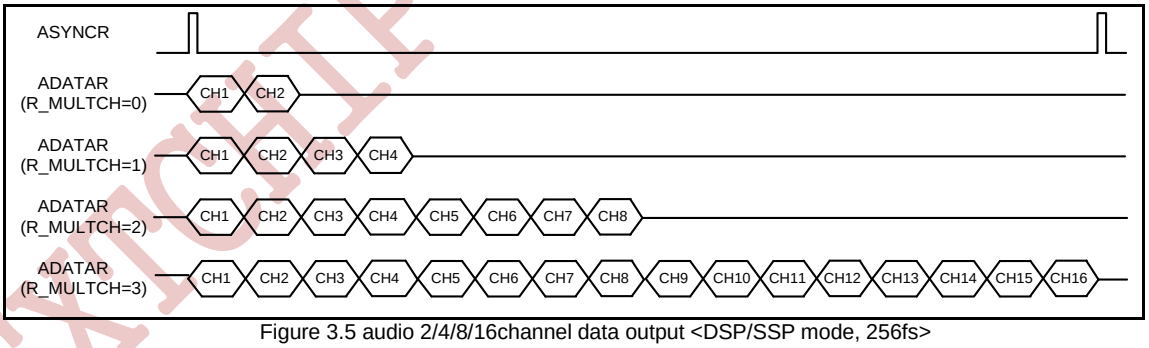


Figure 3.5 audio 2/4/8/16channel data output <DSP/SSP mode, 256fs>

3.1.3 2/4/8/16-Channel Audio Data Output with 4-Channel Mic Data(320 fs)

ADATA_REC supports up to 9 channel(8-Ch audio/1-Ch mic) using single chip and up to 18 channel(16-Ch audio/2-Ch mic) in cascade mode. In this case, the bit-rate of the audio signal should be 320 fs(RM_BITRATE, 0x07[5:4], BANK1).

The number of output channel is configured by internal register value (R_MULTCH, 0x08[1:0], BANK1) and the order of output channel is configured by internal register value (R_SEQ, 0x09 ~ 0x12, / MIC_SEQ, 0x3C ~ 0x3D, BANK1). Therefore, the order of audio output can be changed.

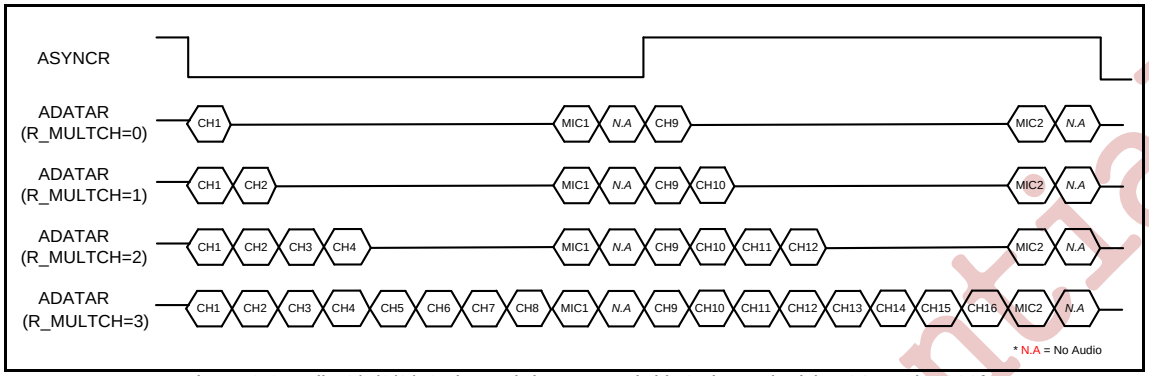


Figure 3.6 audio 2/4/6/8/16 channel data output(with 2 channel mic) <I2S mode, 320fs>

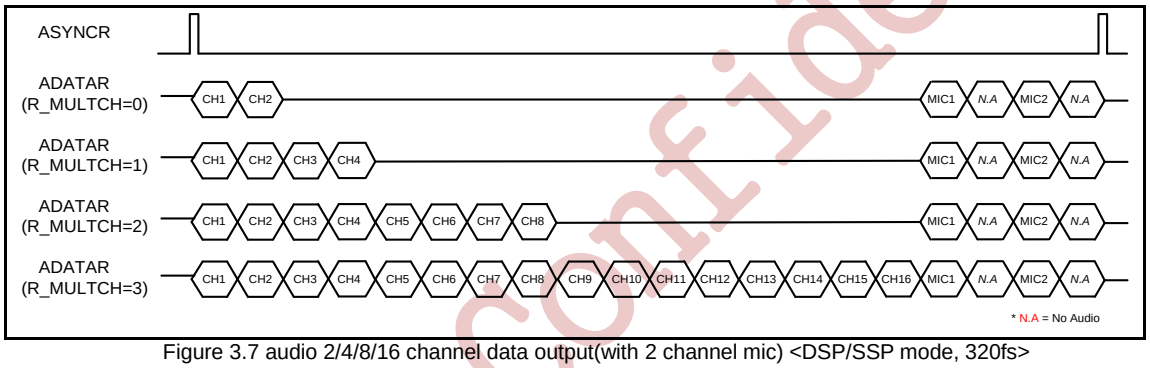


Figure 3.7 audio 2/4/8/16 channel data output(with 2 channel mic) <DSP/SSP mode, 320fs>

3.1.4 ADATA_SP Output

ADATA_SP supports 3 kinds of output method. Firstly, the output data of ADATA_SP pin is the exactly same as those of ADATA_REC except output data sequence. The order of output data is opposite. If the output data order of ADATA_REC is "CH1, CH2, CH9, CH10", the output data order of ADATA_SP is "CH16, CH15, CH8, CH7". That is to say, two output pin - ADATA_SP and ADATA_REC are complement relationship.

Secondly, one of input signals is selected as output signal of ADATA_SP. The selectable input signal ranges from analog input signal to ADATA_PB signal. Lastly, mixed data of input signal is selected as the output signal of ADATA_SP. The mixing gain of each channel's input signal is determined by internal register setting value (MIX_RATIO, 0x16 ~ 0x21[7:0], BANK1).

The output configuration of ADATA_SP is determined by internal register setting. First and second configuration are determined by (R_ADATSP, 0x08[2], BANK1), and second and third configuration are determined by (L_CH_OUTSEL, 0x24[4:0], BANK1) and (R_CH_OUTSEL, 0x25[4:0], BANK1). In this case, L_CH_OUTSEL and R_CH_OUTSEL select one of input channels or mixed data.

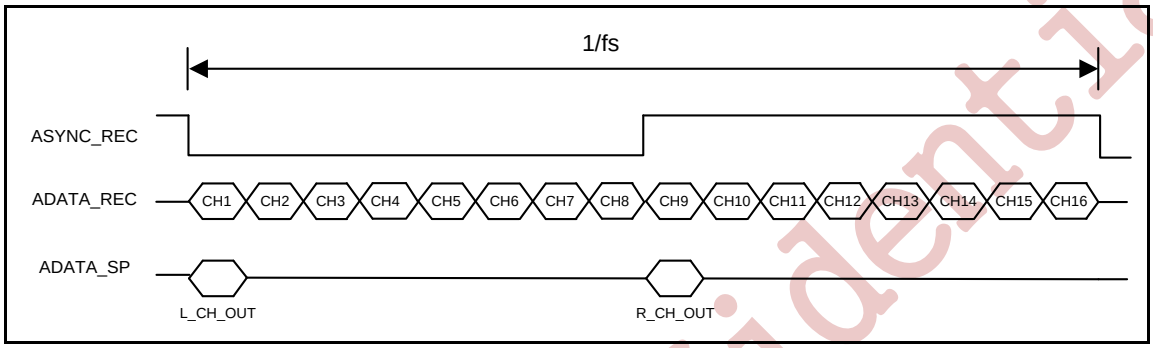


Figure 3.8 ADATA_SP Output <I2S mode>

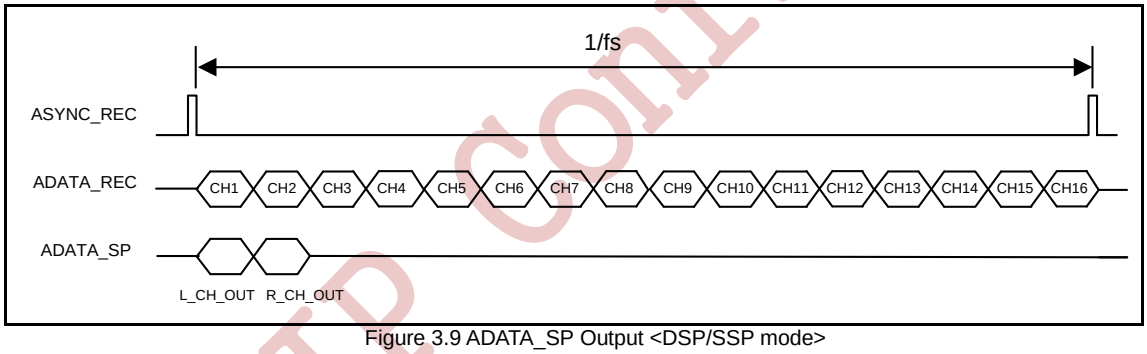


Figure 3.9 ADATA_SP Output <DSP/SSP mode>

3.2 Playback Output

Playback is to output stored audio data to external device through DAC after internal processing.

NVP6134 gives and takes a clock and synchronization signal through ACLK_PB and ASYNC_PB pin. In this case, interface is the exactly same as Record data's interface. When multi-channel audio is supported, selective playback for intended channel is enable using register setting (PB_SER, 0x14[4:0], BANK1). In case of single channel, PB_SEL should be set to "00000".

ACLK_PB and ASYNC_PB supports Master mode and Slave mode. In master mode, ACLK_PB and ASYNC_PB are outputted by **NVP6134**, and clock and synchronization signal come from external devices at slave mode. Master/Slave mode is selected by setting internal register (PB_MASTER, 0x13[7], BANK1).

ADATA_PB accepts an audio data synchronized with ACLK_PB and ASYNC_PB. ACLK_PB and ASYNCP accept I2S/DSP/SSP mode input and output, and I2S and DSP mode is set by internal register value (PB_SYNC, 0x13[0], BANK1). When DSP mode is selected, DSP/SSP mode is set by (PB_SSP, 0x13[1], BANK1). The relation of clock, synchronized signal and data are the exactly same as that of record/mix output. PB_CLK can be inverted for all modes using setting of register(PB_CLK, 0x13[6], BANK1).

3.3 Audio Detection

NVP6134 has an audio mute detection block for individual 9 channels. The mute detection scheme uses absolute/differential amplitude detection method. The detection method and accumulated period are defined by the ADET_MODE(0x29[3], BANK1) and ADET_FILT (0x29[2:0], BANK1) register. According to this control bits and its result (audio detected), Interrupt is generated through the interrupt pins.

3.4 Cascade Operation

NVP6134 supports cascade mode. Maximum 2-**NVP6134** chips can be connected together for cascade mode and can be processed 18 channel audio encoding data(16-Ch Audio/2-Ch mic). Cascade is enabled by setting register(CHIP_STAGE, 0x06[1:0], BANK1). Figure 3.10 shows how to connect **NVP6134** for the cascade mode. In this case, analog audio AOUT1 is assigned to AIN1-16 and MICIN1-4. 1 channel audio or all channel mixed audio signal is selected as output signal set by MIX_OUTSEL(0x23[4:0], BANK1).

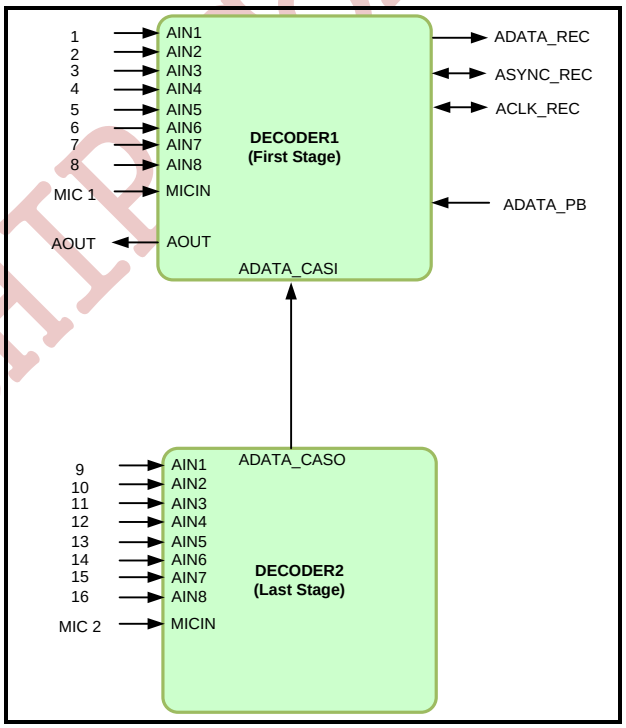


Figure 3.10 Consist of Cascade System using 2-NVP6134

Chapter 4
COAXIAL PROTOCOL

NVP6134 includes Coaxial Protocol generator that sends control signal from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal. **NVP6134** supports Protocol for CVBS/COMET(PELCO) & AHD(A-CP). It depends on Coaxial Cable impedance characteristic. This document presents the concept of Coaxial Protocol. Coaxitron is Pelco's name for a method of sending control signaling from a controller to a pan and tilt, receiver driver, or camera and lens on the video signal (Known as "Up The Coax" or "UTC")

4.1 PELCO PROTOCOL

There are two types of Coaxitron command structures. One type, Standard Coaxitron,. is a series of 15 pulses, or data bits, that are sent within video line 18 of a video field. The other type, Extended Coaxitron, is a series of 32 pulses, where 16 pulses are sent in line 18 and 16 pulses in line 19 of a video field. Refer to Figure 4.1. No pulses are sent when the system is in an idle state

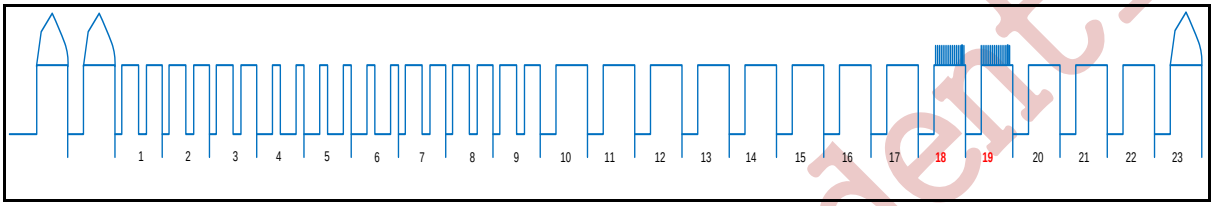


Figure 4.1 Coaxitron Active line

Coaxitron is a pulse width modulated (PWM) That is inserted into video vertical blanking interval. A 2us pulse represents a one(1) and a 1us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 4.2. and Figure 4.3.

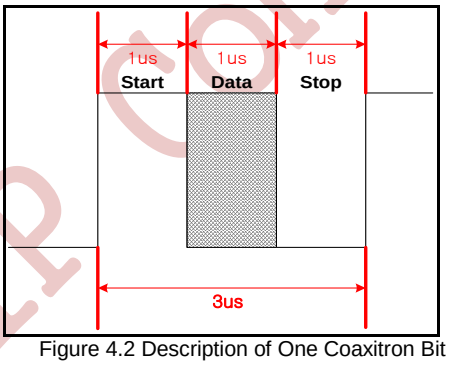


Figure 4.2 Description of One Coaxitron Bit

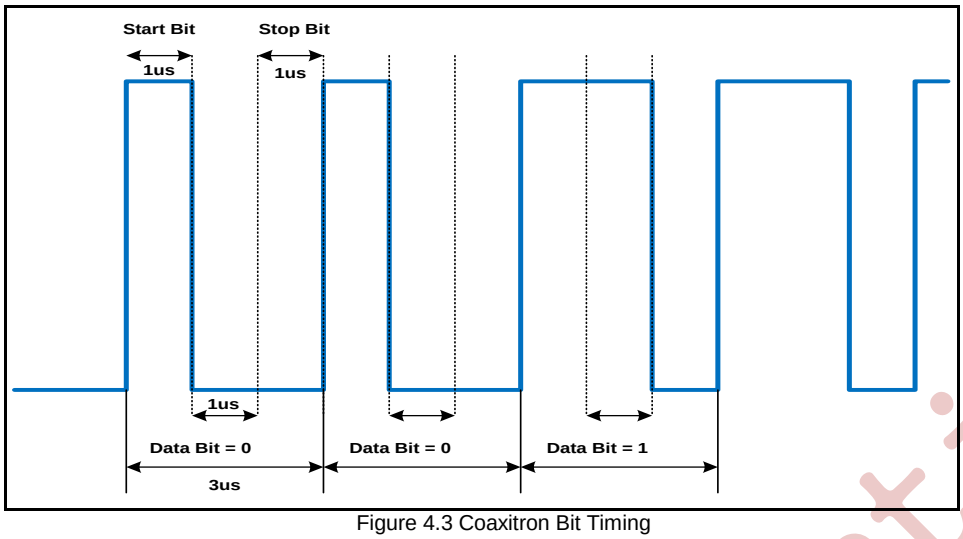


Figure 4.3 Coaxitron Bit Timing

NVP6134 is able to control coaxitron timing format on the video signal.

Start Active line of Coaxitron (BL_TXST, 0x03~04[3:0],0x83~84[3:0], BANK3~4) is 18th line on VBI. Pulse width of Coaxitron (BAUD, 0x00/0x80, BANK3~4) is fixed 1us. The size of Coaxial Data (PELCO_TXDAT, 0x20~23,0xA0~A3, BANK3~4) is 4 bytes. Refer to Figure 4.4.

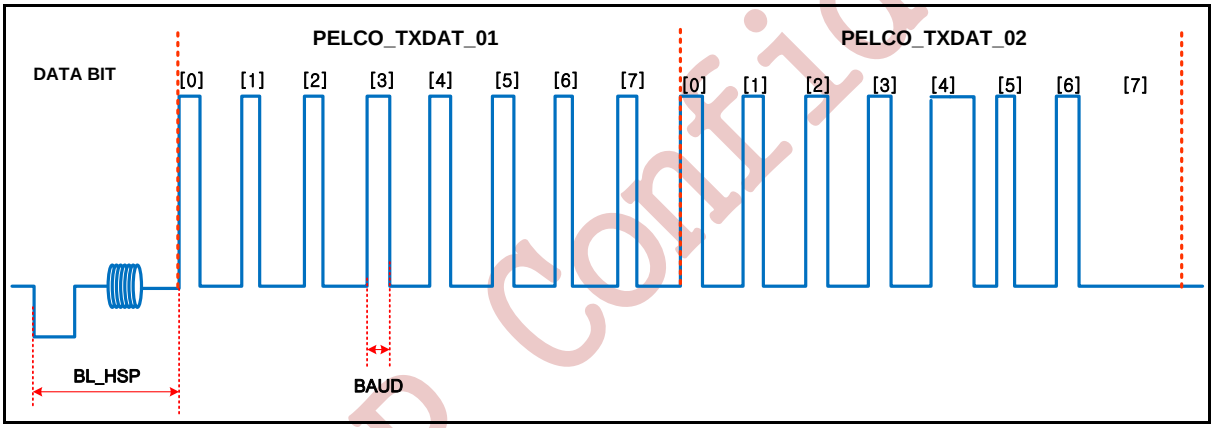


Figure 4.4 Data Structure of Coaxitron Origins (VBI 18th)

4.2 A-CP(AHD-Coaxial protocol)

It is an acronym of AHD Coaxial Protocol. This term signifies the interactive communication protocol between Image Signal Processor. As a major feature, A-CP Data located in the 17~20th line. Also Data is 8bit each line.

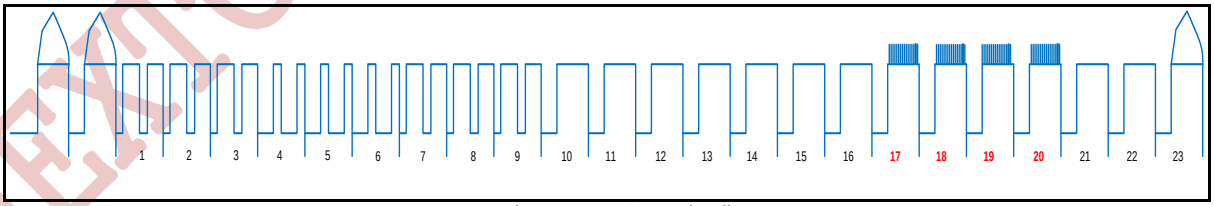


Figure 4.5 A-CP Active line

A-CP is a pulse width modulated (PWM) That is inserted into video vertical blanking interval. A 1.8us pulse represents a one(1) and a 0.6us pulse represents a zero(0). There is a start bit (always high level), a data bit (low or high level) and a stop bit (always low level).

Refer to Figure 4.6. and Figure 4.7.

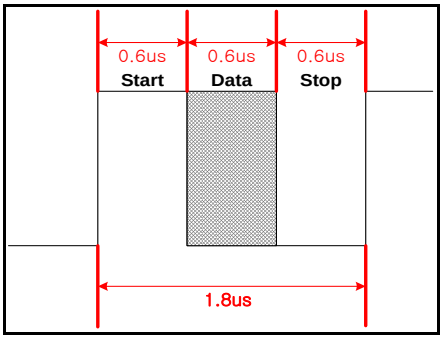


Figure 4.6 Description of A-CP One Data Bit

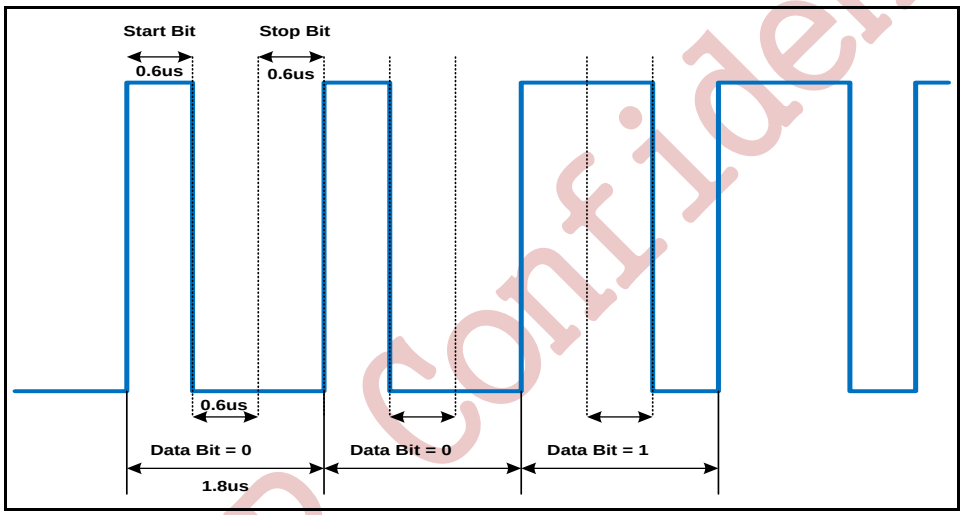


Figure 4.7 Data A-CP Bit Timing

Start Active line of Coaxitron (BL_TXST, 0x0D~0E[3:0],0x8D~8E[3:0], BANK3~4) is 17th line on VBI. Pulse width of Coaxitron (BAUD, 0x00/0x80, BANK3~4) is fixed 0.6us. The size of Coaxial Data (TX_DATA, 0x10~17, 0x90~0x97, BANK3~4) is 4 bytes. Refer to Figure 4.8.

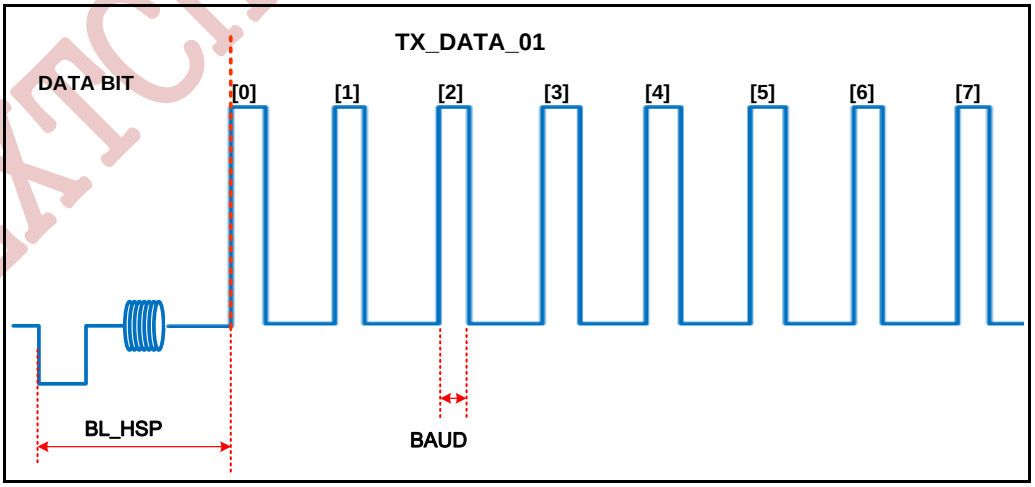


Figure 4.8 Data Structure of Coaxitron Origins (VBI 17th)

Chapter 5
2C INTERFACE

I2C interface requires 2 wires, SCL (I2C clock) & SDA (I2C R/W data). **NVP6134** provides special device ID as slave addresses (SA0, SA1). So any combination of 7 bit can be defined as slave address of **NVP6134**. The Figure 5.1 shows read/write protocol of I2C interface. The 1st byte transfers slave address and read/write information. For write mode, the 2nd byte transfers base register index and the 3rd byte transfers date to be written.

For read mode, reading data is transferred during 2nd byte period. The brief I2C interface protocol is shown in Figure 5.2.

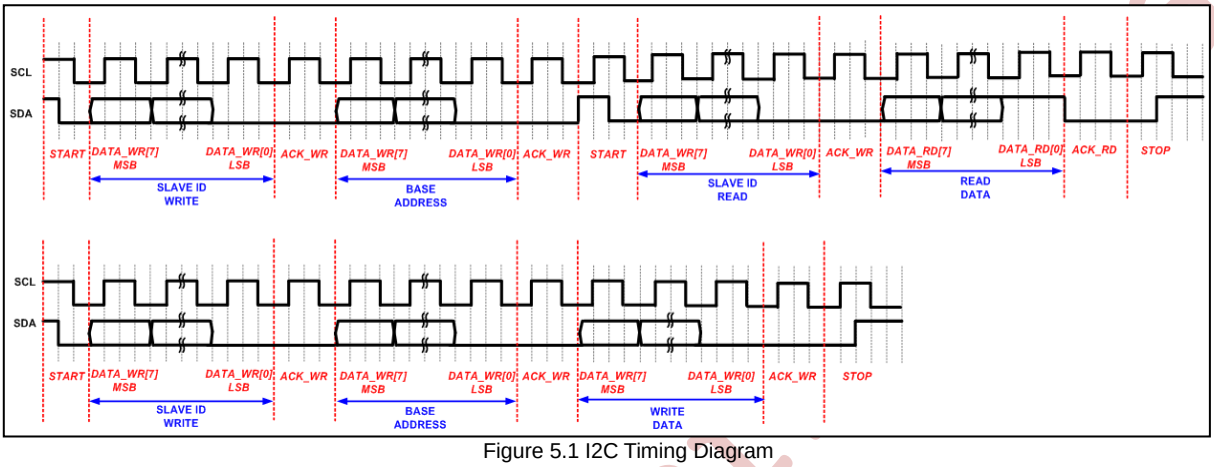


Figure 5.1 I2C Timing Diagram

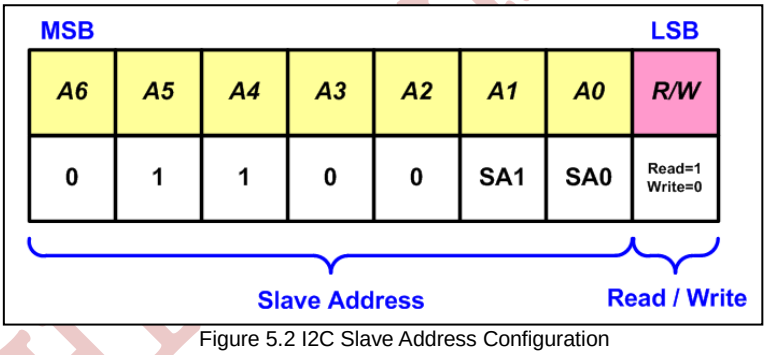


Figure 5.2 I2C Slave Address Configuration

Chapter 6
REGISTER DESCRIPTION

6.1 REGISTER ADDRESS

6.1.1 BANK0 Register(0x00~0x1F) : VIDEO

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK0	0x00				-RESERVED-				PD_VCH1	0x01	0x00	0x00
	0x01				-RESERVED-				PD_VCH2	0x01	0x00	0x00
	0x02				-RESERVED-				PD_VCH3	0x01	0x00	0x00
	0x03				-RESERVED-				PD_VCH4	0x01	0x00	0x00
	0x08	AUTO_1	BSF_MODE_1		VIDEO_FORMAT_1					0x00	0x00	0x00
	0x09	AUTO_2	BSF_MODE_2		VIDEO_FORMAT_2					0x00	0x00	0x00
	0x0A	AUTO_3	BSF_MODE_3		VIDEO_FORMAT_3					0x00	0x00	0x00
	0x0B	AUTO_4	BSF_MODE_4		VIDEO_FORMAT_4					0x00	0x00	0x00
	0x0C	BRIGHTNESS_1								0x08	0xED	0xED
	0x0D	BRIGHTNESS_2								0x08	0xED	0xED
	0x0E	BRIGHTNESS_3								0x08	0xED	0xED
	0x0F	BRIGHTNESS_4								0x08	0xED	0xED
	0x10	CONTRAST_1								0x88	0x88	0x88
	0x11	CONTRAST_2								0x88	0x88	0x88
	0x12	CONTRAST_3								0x88	0x88	0x88
	0x13	CONTRAST_4								0x88	0x88	0x88
	0x14	H_SHARPNESS_1				V_SHARPNESS_1				0x90	0x90	0x90
	0x15	H_SHARPNESS_2				V_SHARPNESS_2				0x90	0x90	0x90
	0x16	H_SHARPNESS_3				V_SHARPNESS_3				0x90	0x90	0x90
	0x17	H_SHARPNESS_4				V_SHARPNESS_4				0x90	0x90	0x90
	0x18	Y_PEAK_MODE_1				Y_FIR_MODE_1				0x00	0x20	0x20
	0x19	Y_PEAK_MODE_2				Y_FIR_MODE_2				0x00	0x20	0x20
	0x1A	Y_PEAK_MODE_3				Y_FIR_MODE_3				0x00	0x20	0x20
	0x1B	Y_PEAK_MODE_4				Y_FIR_MODE_4				0x00	0x20	0x20

6.1.2 BANK0 Register(0x20~0x3F) : VIDEO

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK0	0x21	PAL_CM_OFF_1	IF_FIR_SEL_1			CLPF_SEL_1				0x92	0x92	0x92
	0x22				COLOROFF_1	C_KILL_1				0x0A	0x0B	0x0B
	0x25	PAL_CM_OFF_2	IF_FIR_SEL_2			CLPF_SEL_2				0x92	0x92	0x92
	0x26				COLOROFF_2	C_KILL_2				0x0A	0x0B	0x0B
	0x29	PAL_CM_OFF_3	IF_FIR_SEL_3			CLPF_SEL_3				0x92	0x92	0x92
	0x2A				COLOROFF_3	C_KILL_3				0x0A	0x0B	0x0B
	0x2D	PAL_CM_OFF_4	IF_FIR_SEL_4			CLPF_SEL_4				0x92	0x92	0x92
	0x2E				COLOROFF_4	C_KILL_4				0x0A	0x0B	0x0B
	0x30	-RESERVED-			Y_DELAY_1					0x12	0x10	0x10
	0x31	-RESERVED-			Y_DELAY_2					0x12	0x10	0x10
	0x32	-RESERVED-			Y_DELAY_3					0x12	0x10	0x10
	0x33	-RESERVED-			Y_DELAY_4					0x12	0x10	0x10
	0x34	-RESERVED-	PED_ON_1	-RESERVED-						0x02	0x04	0x02
	0x35	-RESERVED-	PED_ON_2	-RESERVED-						0x02	0x04	0x02
	0x36	-RESERVED-	PED_ON_3	-RESERVED-						0x02	0x04	0x02
	0x37	-RESERVED-	PED_ON_4	-RESERVED-						0x02	0x04	0x02
	0x38	CTI_GAIN_1								0x0A	0x0A	0x0A
	0x39	CTI_GAIN_2								0x0A	0x0A	0x0A
	0x3A	CTI_GAIN_3								0x0A	0x0A	0x0A
	0x3B	CTI_GAIN_4								0x0A	0x0A	0x0A
	0x3C	SATURATION_1								0x90	0x84	0x84
	0x3D	SATURATION_2								0x90	0x84	0x84
	0x3E	SATURATION_3								0x90	0x84	0x84
	0x3F	SATURATION_4								0x90	0x84	0x84

6.1.3 BANK0 Register(0x40~0x5F) : VIDEO

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK0	0x40	HUE_1								0x00	0x00	0x00
	0x41	HUE_2								0x00	0x00	0x00
	0x42	HUE_3								0x00	0x00	0x00
	0x43	HUE_4								0x00	0x00	0x00
	0x44	U_GAIN_1								0x00	0x00	0x00
	0x45	U_GAIN_2								0x00	0x00	0x00
	0x46	U_GAIN_3								0x00	0x00	0x00
	0x47	U_GAIN_4								0x00	0x00	0x00
	0x48	V_GAIN_1								0x00	0x00	0x00
	0x49	V_GAIN_2								0x00	0x00	0x00
	0x4A	V_GAIN_3								0x00	0x00	0x00
	0x4B	V_GAIN_4								0x00	0x00	0x00
	0x4C	U_OFFSET_1								0x00	0x00	0x00
	0x4D	U_OFFSET_2								0x00	0x00	0x00
	0x4E	U_OFFSET_3								0x00	0x00	0x00
	0x4F	U_OFFSET_4								0x00	0x00	0x00
	0x50	V_OFFSET_1								0x00	0x00	0x00
	0x51	V_OFFSET_2								0x00	0x00	0x00
	0x52	V_OFFSET_3								0x00	0x00	0x00
	0x53	V_OFFSET_4								0x00	0x00	0x00
	0x54	FLD_INV_4	FLD_INV_3	FLD_INV_2	FLD_INV_1	NOVID_INF_IN_14	CHID_TYPE_14			0x01	0xF1	0x01
	0x55	CHID_VIN2				CHID_VIN1				0x10	0x10	0x10
	0x56	CHID_VIN4				CHID_VIN3				0x10	0x10	0x10
	0x58	H_DELAY_1								0x80	0x8B	0x80
	0x59	H_DELAY_2								0x80	0x8B	0x80
	0x5A	H_DELAY_3								0x80	0x8B	0x80
	0x5B	H_DELAY_4								0x80	0x8B	0x80
	0x5C	V_DELAY_1								0x00	0x9E	0x9E
	0x5D	V_DELAY_2								0x00	0x9E	0x9E
	0x5E	V_DELAY_3								0x00	0x9E	0x9E
	0x5F	V_DELAY_4								0x00	0x9E	0x9E

6.1.4 BANK0 Register(0x60~0x7F) : VIDEO

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK0	0x60	HBLK_END_1								0x00	0x00	0x00
	0x61	HBLK_END_2								0x00	0x00	0x00
	0x62	HBLK_END_3								0x00	0x00	0x00
	0x63	HBLK_END_4								0x00	0x00	0x00
	0x64	VBLK_END_1								0x00	0xC0	0xC0
	0x65	VBLK_END_2								0x00	0xC0	0xC0
	0x66	VBLK_END_3								0x00	0xC0	0xC0
	0x67	VBLK_END_4								0x00	0xC0	0xC0
	0x68	H_CROP_S_1								0x00	0x00	0x00
	0x69	H_CROP_S_2								0x00	0x00	0x00
	0x6A	H_CROP_S_3								0x00	0x00	0x00
	0x6B	H_CROP_S_4								0x00	0x00	0x00
	0x6C	H_CROP_E_1								0x00	0x00	0x00
	0x6D	H_CROP_E_2								0x00	0x00	0x00
	0x6E	H_CROP_E_3								0x00	0x00	0x00
	0x6F	H_CROP_E_4								0x00	0x00	0x00
	0x70	V_CROP_S_1								0x00	0x00	0x00
	0x71	V_CROP_S_2								0x00	0x00	0x00
	0x72	V_CROP_S_3								0x00	0x00	0x00
	0x73	V_CROP_S_4								0x00	0x00	0x00
	0x74	V_CROP_E_1								0x00	0x00	0x00
	0x75	V_CROP_E_2								0x00	0x00	0x00
	0x76	V_CROP_E_3								0x00	0x00	0x00
	0x77	V_CROP_E_4								0x00	0x00	0x00
	0x78	BGDCOL_2				BGDCOL_1				0x88	0x88	0x88
	0x79	BGDCOL_4				BGDCOL_3				0x88	0x88	0x88
	0x7A	DATA_OUT_MODE_2				DATA_OUT_MODE_1				0x11	0x11	0x11
	0x7B	DATA_OUT_MODE_4				DATA_OUT_MODE_3				0x11	0x11	0x11

6.1.5 BANK0 Register(0x80~0xA3) : VIDEO_ENABLE & Delay

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK0	0x80					EACH_REG_SET				0x00	0x0F	0x0F
	0x81	SD_MD_1				AHD_MD_1				0x03	0x02	0x03
	0x82	SD_MD_2				AHD_MD_2				0x03	0x02	0x03
	0x83	SD_MD_3				AHD_MD_3				0x03	0x02	0x03
	0x84	SD_MD_4				AHD_MD_4				0x03	0x02	0x03
	0x8E	H_DLY_MSB_1				-RESERVED-				0x09	0x00	0x00
	0x8F	H_DLY_MSB_2				-RESERVED-				0x09	0x00	0x00
	0x90	H_DLY_MSB_3				-RESERVED-				0x09	0x00	0x00
	0x91	H_DLY_MSB_4				-RESERVED-				0x09	0x00	0x00
	0x93	-RESERVED-							HZOOM_ON_1	0x00	0x00	0x00
	0x94	-RESERVED-							HZOOM_ON_2	0x00	0x00	0x00
	0x95	-RESERVED-							HZOOM_ON_3	0x00	0x00	0x00
	0x96	-RESERVED-							HZOOM_ON_4	0x00	0x00	0x00
	0x97	-RESERVED-								0x00	0x00	0x00
	0x98	-RESERVED-				H_ZOOM_DTO_1				0x07	0x00	0x00
	0x99	-RESERVED-				H_ZOOM_DTO_2				0x07	0x00	0x00
	0x9A	-RESERVED-				H_ZOOM_DTO_3				0x07	0x00	0x00
	0x9B	-RESERVED-				H_ZOOM_DTO_4				0x07	0x00	0x00
	0xA0	DF_CDELAY_1				DF_YDELAY_1				0x00	0x00	0x00
	0xA1	DF_CDELAY_2				DF_YDELAY_2				0x00	0x00	0x00
	0xA2	DF_CDELAY_3				DF_YDELAY_3				0x00	0x00	0x00
	0xA3	DF_CDELAY_4				DF_YDELAY_4				0x00	0x00	0x00

6.1.6 BANK0 Register(0xA8~0xF5) : STATUS

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK0	0xA8					NOVID_04	NOVID_03	NOVID_02	NOVID_01	R	R	R
	0xA9					MOTION_04	MOTION_03	MOTION_02	MOTION_01	R	R	R
	0xAC	MUTE_08	MUTE_07	MUTE_06	MUTE_05	MUTE_04	MUTE_03	MUTE_02	MUTE_01	R	R	R
	0xAD	MUTE_16	MUTE_15	MUTE_14	MUTE_13	MUTE_12	MUTE_11	MUTE_10	MUTE_09	R	R	R
	0xAE							MUTEMIC_02	MUTEMIC_01	R	R	R
	0xAF					COAX_RX_DONE_4	COAX_RX_DONE_3	COAX_RX_DONE_2	COAX_RX_DONE_1	R	R	R
	0xB0					NOVID_04B	NOVID_03B	NOVID_02B	NOVID_01B	R	R	R
	0xB1					MOTION_04B	MOTION_03B	MOTION_02B	MOTION_01B	R	R	R
	0xB4	MUTE_08B	MUTE_07B	MUTE_06B	MUTE_05B	MUTE_04B	MUTE_03B	MUTE_02B	MUTE_01B	R	R	R
	0xB5	MUTE_16B	MUTE_15B	MUTE_14B	MUTE_13B	MUTE_12B	MUTE_11B	MUTE_10B	MUTE_09B	R	R	R
	0xB6							MUTEMIC_02B	MUTEMIC_01B	R	R	R
	0xB7					COAX_RX_DONE_4B	COAX_RX_DONE_3B	COAX_RX_DONE_2B	COAX_RX_DONE_1B	R	R	R
	0xB8	RD_STATE_CLR			STATE_HOLD					0x90	0x90	0x90
	0xB9				IRQ_MSB	IRQ_INV	IRQ_SEL			0x00	0x00	0x00
	0xE0					AGC_LOCK_04	AGC_LOCK_03	AGC_LOCK_02	AGC_LOCK_01	R	R	R
	0xE1					CMP_LOCK_04	CMP_LOCK_03	CMP_LOCK_02	CMP_LOCK_01	R	R	R
	0xE2					H_LOCK_04	H_LOCK_03	H_LOCK_02	H_LOCK_01	R	R	R
	0xE7					BW_04	BW_03	BW_02	BW_01	R	R	R
	0xE8	-RESERVED-				FSC_CHG_DONE_01	CKILL_01	FSC_LOCK_DONE_01	NOVIDEO_01	R	R	R
	0xE9	-RESERVED-				FSC_CHG_DONE_02	CKILL_02	FSC_LOCK_DONE_02	NOVIDEO_02	R	R	R
	0xEA	-RESERVED-				FSC_CHG_DONE_03	CKILL_03	FSC_LOCK_DONE_03	NOVIDEO_03	R	R	R
	0xEB	-RESERVED-				FSC_CHG_DONE_04	CKILL_04	FSC_LOCK_DONE_04	NOVIDEO_04	R	R	R
	0xF4	DEV_ID (NVP6134 = 0x91)								R	R	R
	0xF5	REV_ID (0x01)								R	R	R

6.1.7 BANK1 Register(0x00~0x1F) : AUDIO

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK1	0x00	PD_AU_AFE	PD_AU_DAC			RM_PB_PIN	PB_RM_PIN	FILTER_ON	EN_32K_ MODE	0x02	0x02	0x02
	0x01	AIGAIN_01								0x00	0x08	0x08
	0x02	AIGAIN_02								0x00	0x08	0x08
	0x03	AIGAIN_03								0x00	0x08	0x08
	0x04	AIGAIN_04								0x00	0x08	0x08
	0x05	MIGAIN_01								0x00	0x08	0x08
	0x06	CAS_PB	TRANS_MODE	-	CAS_PIN	CASCADE_ MODE	*-RESERVED-*	CHIP_STAGE		0x1B	0x1B	0x1B
	0x07	RM_MASTER	RM_CLK	RM_BITRATE		RM_SAMRATE	RM_BITWID	RM_SSP	RM_SYNC	0xC8	0xC8	0xC8
	0x08	RM_BIT_ SWAP	RM_LAW_SEL	RM_FORMAT		*-RESERVED-*	R_ADATSP	R_MULTCH		0x03	0x03	0x03
	0x09	R_SEQ_08[4]	R_SEQ_07[4]	R_SEQ_06[4]	R_SEQ_05[4]	R_SEQ_04[4]	R_SEQ_03[4]	R_SEQ_02[4]	R_SEQ_01[4]	0x00	0x00	0x00
	0x0A	R_SEQ_02[3:0]				R_SEQ_01[3:0]				0x10	0x10	0x10
	0x0B	R_SEQ_04[3:0]				R_SEQ_03[3:0]				0x32	0x32	0x32
	0x0C	R_SEQ_06[3:0]				R_SEQ_05[3:0]				0x54	0x54	0x54
	0x0D	R_SEQ_08[3:0]				R_SEQ_07[3:0]				0x76	0x76	0x76
	0x0E	R_SEQ_16[4]	R_SEQ_15[4]	R_SEQ_14[4]	R_SEQ_13[4]	R_SEQ_12[4]	R_SEQ_11[4]	R_SEQ_10[4]	R_SEQ_09[4]	0x00	0x00	0x00
	0x0F	R_SEQ_10[3:0]				R_SEQ_09[3:0]				0x98	0x98	0x98
	0x10	R_SEQ_12[3:0]				R_SEQ_11[3:0]				0xBA	0xBA	0xBA
	0x11	R_SEQ_14[3:0]				R_SEQ_13[3:0]				0xDC	0xDC	0xDC
	0x12	R_SEQ_16[3:0]				R_SEQ_15[3:0]				0xFE	0xFE	0xFE
	0x13	PB_MASTER	PB_CLK	PB_BITRATE		PB_SAMRATE	PB_BITWID	PB_SSP	PB_SYNC	0x08	0x08	0x08
	0x14	PB_BIT_ SWAP	-	PB_SEL						0x00	0x00	0x00
	0x15	PB_FORMAT		-		PB_ LAW_SEL	*-RESERVED-*			0x00	0x00	0x00
	0x16	MIX_RATIO_02				MIX_RATIO_01				0x88	0x88	0x88
	0x17	MIX_RATIO_04				MIX_RATIO_03				0x88	0x88	0x88
	0x18	MIX_RATIO_06				MIX_RATIO_05				0x88	0x88	0x88
	0x19	MIX_RATIO_08				MIX_RATIO_07				0x88	0x88	0x88
	0x1A	MIX_RATIO_10				MIX_RATIO_09				0x88	0x88	0x88
	0x1B	MIX_RATIO_12				MIX_RATIO_11				0x88	0x88	0x88
	0x1C	MIX_RATIO_14				MIX_RATIO_13				0x88	0x88	0x88
	0x1D	MIX_RATIO_16				MIX_RATIO_15				0x88	0x88	0x88
	0x1E	MIX_RATIO_M2				MIX_RATIO_M1				0x88	0x88	0x88

6.1.8 BANK1 Register(0x20~0x44) : AUDIO

	ADDRESS	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK1	0x20	MIX_RATIO_P2				MIX_RATIO_P1				0x88	0x88	0x88
	0x21	MIX_RATIO_P4				MIX_RATIO_P3				0x88	0x88	0x88
	0x22	AOGAIN								0x00	0x08	0x08
	0x23	-		MIX_DERATIO	MIX_OUTSEL					0x19	0x19	0x19
	0x24	-			L_CH_OUTSEL					0x18	0x19	0x19
	0x25	-			R_CH_OUTSEL					0x16	0x19	0x19
	0x26	MIX_MUTE_08	MIX_MUTE_07	MIX_MUTE_06	MIX_MUTE_05	MIX_MUTE_04	MIX_MUTE_03	MIX_MUTE_02	MIX_MUTE_01	0x00	0x00	0x00
	0x27	MIX_MUTE_16	MIX_MUTE_15	MIX_MUTE_14	MIX_MUTE_13	MIX_MUTE_12	MIX_MUTE_11	MIX_MUTE_10	MIX_MUTE_09	0x00	0x00	0x00
	0x28	-RESERVED-		MIX_MUTE_M2	MIX_MUTE_M1	MIX_MUTE_P4	MIX_MUTE_P3	MIX_MUTE_P2	MIX_MUTE_P1	0x00	0x00	0x00
	0x29	AUTO_MUTE	-RESERVED-			ADET_MODE	ADET_FILT			0x88	0x88	0x88
	0x2A	ADET_08	ADET_07	ADET_06	ADET_05	ADET_04	ADET_03	ADET_02	ADET_01	0xFF	0xFF	0xFF
	0x2B	-	ADET_M1	-						0xC0	0x40	0x40
	0x38	-RESERVED-			AUD_SW_RST	-RESERVED-				0x08	0x08	0x08
	0x3A					A_DAC_GAIN				0xA2	0x03	0x03
	0x3B	A_GAIN_SEL(AFE)				-RESERVED-				0x30	0x30	0x30
	0x3C	-			MIC_SEQ_01					0x00	0x10	0x10
	0x3D	-			MIC_SEQ_02					0x00	0x11	0x11
	0x40	AIGAIN_05								0x00	0x08	0x08
	0x41	AIGAIN_06								0x00	0x08	0x08
	0x42	AIGAIN_07								0x00	0x08	0x08
	0x43	AIGAIN_08								0x00	0x08	0x08

6.1.9 BANK1 Register(0x80~0x9F) : IP Power Down

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK1	0x97					CH_RST4	CH_RST3	CH_RST2	CH_RST1	0x0F	0x0F	0x0F
	0x98					PD_DEC4	PD_DEC3	PD_DEC2	PD_DEC1	0x00	0x00	0x00
	0x9A				AU_RST				PD_AUD	0x00	0x00	0x00

6.1.10 BANK1 Register(0xB0~0xBF) : MPP

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK1	0xB1					MPP4_DIR	MPP3_DIR	MPP2_DIR	MPP1_DIR	0x00	0x00	0x00
	0xB2					MPP4_CLK	MPP3_CLK	MPP2_CLK	MPP1_CLK	0x00	0x00	0x00
	0xB3					MPP4_INV	MPP3_INV	MPP2_INV	MPP1_INV	0x00	0x00	0x00
	0xB4	MPP_CLK1_SEL				MPP_CLK1_DLY_SEL				0x40	0x40	0x40
	0xB5	MPP_CLK2_SEL				MPP_CLK2_DLY_SEL				0x40	0x40	0x40
	0xB6	MPP_CLK3_SEL				MPP_CLK3_DLY_SEL				0x40	0x40	0x40
	0xB7	MPP_CLK4_SEL				MPP_CLK4_DLY_SEL				0x40	0x40	0x40

6.1.11 BANK1 Register(0xC0~0xCF) : OUTPUT PORT

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK1	0xC0	VPORT_1_SEQ2				VPORT_1_SEQ1				0x00	0x00	0x00
	0xC1	VPORT_1_SEQ4				VPORT_1_SEQ3				0x00	0x00	0x00
	0xC2	VPORT_2_SEQ2				VPORT_2_SEQ1				0x11	0x11	0x11
	0xC3	VPORT_2_SEQ4				VPORT_2_SEQ3				0x11	0x11	0x11
	0xC4	VPORT_3_SEQ2				VPORT_3_SEQ1				0x22	0x22	0x22
	0xC5	VPORT_3_SEQ4				VPORT_3_SEQ3				0x22	0x22	0x22
	0xC6	VPORT_4_SEQ2				VPORT_4_SEQ1				0x33	0x33	0x33
	0xC7	VPORT_4_SEQ4				VPORT_4_SEQ3				0x33	0x33	0x33
	0xC8	VPORT_2_CH_OUT_SEL				VPORT_1_CH_OUT_SEL				0x00	0x00	0x00
	0xC9	VPORT_4_CH_OUT_SEL				VPORT_3_CH_OUT_SEL				0x00	0x00	0x00
	0xCA	VCLK_4_EN	VCLK_3_EN	VCLK_2_EN	VCLK_1_EN	VDO_4_EN	VDO_3_EN	VDO_2_EN	VDO_1_EN	0x00	0xFF	0xFF
	0xCB	-RESERVED-				OUT_DATA_4_INV	OUT_DATA_3_INV	OUT_DATA_2_INV	OUT_DATA_1_INV	0x00	0x00	0x00
	0xCC	VPORT_1_OCLK_SEL				VPORT_1_OVCLK _DLY_SEL				0x46	0x46	0x46
	0xCD	VPORT_2_OCLK_SEL				VPORT_2_OVCLK _DLY_SEL				0x46	0x46	0x46
	0xCE	VPORT_3_OCLK_SEL				VPORT_3_OVCLK _DLY_SEL				0x46	0x46	0x46
	0xCF	VPORT_4_OCLK_SEL				VPORT_4_OVCLK _DLY_SEL				0x46	0x46	0x46

6.1.12 BANK2 Register(0x00~0x1F) : MOTION

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	FHD	HD
BANK2	0x00	-RESERVED-				CH1_MOTION_PIC		-RESERVED-	CH1_MOTION_OFF	0x0D	0xED	0x09
	0x01	CH1_MOD_TSEN								0x60	0x60	0x60
	0x02	-RESERVED-					CH1_MOD_PSEN			0x23	0x88	0x88
	0x07	-RESERVED-				CH2_MOTION_PIC		-RESERVED-	CH2_MOTION_OFF	0x0D	0x0D	0x0D
	0x08	CH2_MOD_TSEN								0x60	0x60	0x60
	0x0E	-RESERVED-				CH3_MOTION_PIC		-RESERVED-	CH3_MOTION_OFF	0x0D	0x0D	0x0D
	0x0F	CH3_MOD_TSEN								0x60	0x60	0x60
	0x15	-RESERVED-				CH4_MOTION_PIC		-RESERVED-	CH4_MOTION_OFF	0x0D	0x0D	0x0D
	0x16	CH4_MOD_TSEN								0x60	0x60	0x60

6.1.13 BANK3~4 Register(0x00~0x7F / 0x80~0xFF) : COAXIAL

ADDRESS		REGISTER NAME
Bank	Addr	
3	0x00 ~ 0x7F	Coaxial CH1
3	0x80 ~ 0xFF	Coaxial CH2
4	0x00 ~ 0x7F	Coaxial CH3
4	0x80 ~ 0xFF	Coaxial CH4

6.1.14 BANK3~4 Register(0x00~0x1F / 0x80~0x9F) : COAXIAL CH1~4

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK3/4	0x00	CH1_BAUD								0x37	0x27	0x27
	0x02	CH1_PELCO_BAUD								0x1B	0x1B	0x1B
	0x03	CH1_BL_TXST[7:0]								0x05	0x0E	0x0E
	0x04	CH1_BL_TXST[15:8]								0x00	0x00	0x00
	0x05					CH1_ACT_LEN				0x00	0x03	0x03
	0x07	CH1_PELCO_TXST[7:0]								0x00	0x0E	0x0E
	0x08	CH1_PELCO_TXST[15:8]								0x00	0x00	0x00
	0x09	-			CH1_COAX_SW_RST	CH1_CNT_MODE			CH1_TX_START	0x00	0x08	0x08
	0x0A	-			CH1_TX_BYTE_LENGTH					0x08	0x03	0x03
	0x0B	CH1_PELCO_8BIT	-RESERVED-		CH1_LINE_8BIT	-RESERVED-	CH1_PACKET_MODE			0x06	0x10	0x10
	0x0C	-							CH1_PELCO_CTEN	0x00	0x00	0x00
	0x0D	CH1_BL_HSP[7:0]								0x46	0xB4	0x48
	0x0E	CH1_BL_HSP[15:8]								0x00	0x00	0x02
	0x0F	-							CH1_PELCO_SHOT	0x00	0x00	0x00
	0x10	CH1_TX_DATA_01								0xAA	0x00	0x00
	0x11	CH1_TX_DATA_02								0x1C	0x10	0x10
	0x12	CH1_TX_DATA_03								0x18	0x18	0x18
	0x13	CH1_TX_DATA_04								0xFF	0xFF	0xFF
	0x14	CH1_TX_DATA_05								0xAA	0xAA	0xAA
	0x15	CH1_TX_DATA_06								0x3C	0x3C	0x3C
	0x16	CH1_TX_DATA_07								0xFF	0xFF	0xFF
	0x17	CH1_TX_DATA_08								0xFF	0xFF	0xFF
	0x18	CH1_TX_DATA_09								0xAA	0xAA	0xAA
	0x19	CH1_TX_DATA_10								0x1B	0x1B	0x1B
	0x1A	CH1_TX_DATA_11								0x00	0x00	0x00
	0x1B	CH1_TX_DATA_12								0x00	0x00	0x00
	0x1C	CH1_TX_DATA_13								0xAA	0xAA	0xAA
	0x1D	CH1_TX_DATA_14								0x3B	0x3B	0x3B
	0x1E	CH1_TX_DATA_15								0x00	0x00	0x00
	0x1F	CH1_TX_DATA_16								0x00	0x00	0x00

6.1.15 BANK3~4 Register(0x20~0x5F / 0xA0~0xDF) : COAXIAL CH1~4

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK3/4	0x20	CH1_PELCO_TXDAT_01								0x00	0x00	0x00
	0x21	CH1_PELCO_TXDAT_02								0x00	0x00	0x00
	0x22	CH1_PELC O_TXDAT_03								0x00	0x00	0x00
	0x23	CH1_PELCO_TXDAT_04								0x00	0x00	0x00
	0x2C	CH1_VSO_INV								0x00	0x00	0x00
	0x2D	CH1_HSO_INV								0x00	0x00	0x00
	0x2F	CH1_ EVEN_SUM								0x01	0x00	0x00
	0x3A								CH1_CLEAN	0x00	0x00	0x00
	0x50	CH1_PELCO_8_00								R	R	R
	0x51	CH1_PELCO_8_01								R	R	R
	0x52	CH1_PELCO_8_02								R	R	R
	0x53	CH1_PELCO_8_03								R	R	R
	0x54	CH1_PELCO_8_04								R	R	R
	0x55	CH1_PELCO_8_05								R	R	R
	0x56	CH1_PELCO_8_06								R	R	R
	0x57	CH1_PELCO_8_07								R	R	R
	0x5C								CH1_ RX_DONE	R	R	R
	0x5D	CH1_RX_COAX_DUTY								R	R	R

6.1.16 BANK3~4 Register(0x60~0x79 / 0xE0~0xF9) : COAXIAL CH1~4

ADDRESS		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	Def.	30P	25P
BANK3/4	0x60	CH1_DEVICE_ID								0x00	0x48	0x48
	0x62	CH1_RX_AREA								0x00	0x06	0x06
	0x63				CH1_DELAY_ON				CH1_COMM_ON	0x00	0x01	0x01
	0x64	CH1_DELAY_CNT								0x00	0x00	0x00
	0x65								CH1_MSB	0x00	0x01	0x01
	0x66	CH1_A_DUTY_ON	-RESERVED-							0x00	0x80	0x80
	0x67								CH1_INT_MODE	0x00	0x01	0x01
	0x68	CH1_RX_SZ								0x00	0x50	0x50
	0x69	CH1_M_DUTY								0x00	0x00	0x00
	0x6A	CH1_RX_START_POSITION								0x00	0x00	0x00
	0x6C	CH1_PELCO16_00 [7:0]								R	R	R
	0x6D	CH1_PELCO16_00 [15:8]								R	R	R
	0x6E	CH1_PELCO16_01 [7:0]								R	R	R
	0x6F	CH1_PELCO16_01 [15:8]								R	R	R
	0x70	CH1_PELCO16_02[7:0]								R	R	R
	0x71	CH1_PELCO16_02[15:8]								R	R	R
	0x72	CH1_PELCO16_03[7:0]								R	R	R
	0x73	CH1_PELCO16_03[15:8]								R	R	R
	0x74	CH1_PELCO16_04[7:0]								R	R	R
	0x75	CH1_PELCO16_04[15:8]								R	R	R
	0x76	CH1_PELCO16_05[7:0]								R	R	R
	0x77	CH1_PELCO16_0515:8]								R	R	R
	0x78	CH1_PELCO16_06[7:0]								R	R	R
	0x79	CH1_PELCO16_06[15:8]								R	R	R

*** Registers of Bank 5 ~ Bank 10 are not for users.**

6.2 Register Detail Description

6.2.1 VIDEO Registers

- **Registers to Power Down Mode**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x00	PD_VCH1	[0]	0x0		**PD_VCH1 :** Power down for CH1 Video AFE **PD_VCH2 :** Power down for CH2 Video AFE **PD_VCH3 :** Power down for CH3 Video AFE **PD_VCH4 :** Power down for CH4 Video AFE **0 :** Normal Operation **1 :** Power Down
	0x01	PD_VCH2	[0]			
	0x02	PD_VCH3	[0]			
	0x03	PD_VCH4	[0]			

- **Registers to Control Comb Filter and Video Format**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x08	AUTO_1	[7]	SD : 0xA0 / Others : 0x00	SD : 0xDD / Others : 0x00	**AUTO_x** : A register to set the Auto Detect Mode On/Off; When the AUTO mode has a high value, the Auto_NT_x bit value of the STATUS Register(BANK0, 0xEF]) is to be confirmed to distinguish NTSC-M/J and PAL-B/D/G/H standards. It does not support other standards, and when used in link with the DVR controller, it cannot be used in the NON_REAL_TIME mode. (x = channel 1~4). **0 :** Auto Detect OFF **1 :** Auto Detect ON
	0x09	AUTO_2				
	0x0A	AUTO_3				
	0x0B	AUTO_4				
	0x08	BSF_MODE_1	[6:5]			**BSF_MODE_x :** Selects the filter to make primary separation of the brightness and color signals. (x = channel 1~4) **00 :** LPF Auto Mode **01 :** Mode 1 (2.7~5.4MHz Cut-off) **10 :** Mode 2 (3.5~5.6MHz Cut-off) **11 :** Manual(BANKA~B,0x60 ~ 0x72, 0xD0 ~ 0xE2)
	0x09	BSF_MODE_2				
	0x0A	BSF_MODE_3				
	0x0B	BSF_MODE_4				
	0x08	VIDEO_FORMAT_1	[4:0]			**VIDEO_FORMAT_x :** A register to determine the video standards of the input signal (x = channel 1~4) **00000 :** NTSC-M,J **10001 :** NTSC-4.43 **11101 :** PAL-B,D,G,H,I **10110 :** PAL-M **11111 :** PAL-Nc **10101 :** PAL-60 **Others :** None
	0x09	VIDEO_FORMAT_2				
	0x0A	VIDEO_FORMAT_3				
	0x0B	VIDEO_FORMAT_4				

Registers to Control Luminance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x0C	BRIGHTNESS_1	[7:0]	0xED	0xED	**BRIGHTNESS_x :** Brightness control; DC level of the Luma signal is adjustable up to -128 ~ +127. BRIGHTNESS consists of 2's Complements. (x = channel 1~4) **00000001** : + 1 **01111111** : + 127 **10000000** : - 128 **11111111** : - 1
	0x0D	BRIGHTNESS_2				
	0x0E	BRIGHTNESS_3				
	0x0F	BRIGHTNESS_4				

Registers to Control Contrast

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x10	CONTRAST_1	[7:0]	0x88	0x88	**CONTRAST_x :** Contrast control, Gain level of the Luma signal is adjustable up to x2. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4) **00000000** : ≒ x 0 **01000000** : ≒ x 0.5 **10000000** : ≒ x 1 **11111111** : ≒ x 2
	0x11	CONTRAST_2				
	0x12	CONTRAST_3				
	0x13	CONTRAST_4				

Registers to Control Sharpness

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x14	H_SHARPNESS_1	[7:4]	SD : 0x80 / Others : 0x90		**H_SHARPNESS_x :** Selects the H_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4) **0000** : x 0 **0100** : x 0.5 **1000** : x 1 **1111** : x 2
	0x15	H_SHARPNESS_2				
	0x16	H_SHARPNESS_3				
	0x17	H_SHARPNESS_4				
	0x14	V_SHARPNESS_1	[3:0]			**V_SHARPNESS_x :** Selects the V_Sharpness Value to calculate the brightness information. It consists of four bits in total. MSB represents an integral number while the rest the decimal fraction. (x = channel 1~4) **0000** : x 1 **0100** : x 2 **1000** : x 3 **1111** : x 4
	0x15	V_SHARPNESS_2				
	0x16	V_SHARPNESS_3				
	0x17	V_SHARPNESS_4				

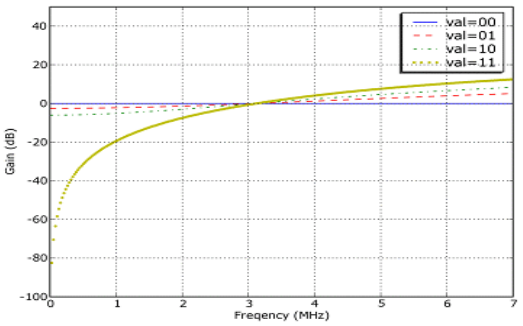
Registers to Control Peaking Filter

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x18	Y_PEAK_MODE_1	[7:4]	SD : 0x0 / Others : 0x2		**Y_PEAK_MODE_x :** Y Peaking Filter control (x = channel 1~4) **0000** : 0dB **0001** : 2dB **0010** : 3.5dB **0011** : 6dB **0100 ~ 1111 :** Don't use
	0x19	Y_PEAK_MODE_2	[7:4]			
	0x1A	Y_PEAK_MODE_3	[7:4]			
	0x1B	Y_PEAK_MODE_4	[7:4]			

Registers to Control Low Pass Filter

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x18	Y_FIR_MODE_1	[3:0]	SD720H : 0x4 / SD960H : 0x8 / Others : 0x0		**Y_FIR_MODE_x :** Y Low Pass Filter control (x = channel 1~4) **0000** : bypass **0101** : 8MHz **0001** : 6MHz **0110** : 8.5MHz **0010** : 6.5MHz **1000** : 9.5MHz **0011** : 7MHz **0111** : 9MHz **0100** : 7.5MHz **etc** : Manual(BANK**A**~BANK**B**, 0x54~0x5A, 0xD4~0xDA)
	0x19	Y_FIR_MODE_2	[3:0]			
	0x1A	Y_FIR_MODE_3	[3:0]			
	0x1B	Y_FIR_MODE_4	[3:0]			

Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x21	PAL_CM_OFF_1	[7]	SD : 0x82 Others : 0x92	SD : 0x02 Others : 0x92	**PAL_CM_OFF_x** (x = channel 1~4) **:** PAL Compensation On/Off. **0** : PAL Compensation applied **1** : PAL Compensation not applied.
	0x25	PAL_CM_OFF_2				
	0x29	PAL_CM_OFF_3				
	0x2D	PAL_CM_OFF_4				
	0x21	IF_FIR_SEL_1	[6:4]			**IF_FIR_SEL_x** (x = channel 1~4) **:** IF Filter drive mode selected. **000** : bypass **001** : mode1 **010** : mode2 **Others** : mode3 
	0x25	IF_FIR_SEL_2				
	0x29	IF_FIR_SEL_3				
	0x2D	IF_FIR_SEL_4				
	0x21	CLPF_SEL_1	[3:0]			**CLPF_SEL_x** (x = channel 1~4) **:** C low pass filter applied mode applied after color demodulation. **0000 :** Bypass **0001 :** 0.6MHz cut off **0010 :** 1.0MHz cut off **0011 :** 1.2MHz cut off **Others :** Bypass
	0x25	CLPF_SEL_2				
	0x29	CLPF_SEL_3				
	0x2D	CLPF_SEL_4				

Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x22	COLOROFF_1	[4]	0x0B	0x0B	**COLOROFF_x** (x = channel 1~4) **:** COLOR OFF **0 :** Color ON **1 :** Color OFF
	0x26	COLOROFF_2	[4]			
	0x2A	COLOROFF_3	[4]			
	0x2E	COLOROFF_4	[4]			
	0x22	C_KILL_1	[3:0]			**C_KILL_x[3]** (x = channel 1~4) **:** Select to Color kill mode **0 :** Not Y/C separation **1 :** Color kill after Y/C separation **C_KILL_x[2:0]** (x = channel 1~4) **:** color kill control. **000 :** Burst Amplitude 10% Under & FSC Unlock **001 :** Burst Amplitude 5% Under & FSC Unlock **010 :** Burst Amplitude 10 % Under **011 :** Burst Amplitude 5% Under **100 :** Always color on **101 :** Always color on. **110 :** Always color off **111 :** Always color off
	0x26	C_KILL_2				
	0x2A	C_KILL_3				
	0x2E	C_KILL_4				

Registers to Control Y_DELAY

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x30	Y_DELAY_1	[4:0]	0x10	0x10	**Y_DELAY_ ON_x** (x = channel 1~4) **:** Y DELAY Control, controllable between 0x00 ~ 0x1F.
	0x31	Y_DELAY_2				
	0x32	Y_DELAY_3				
	0x33	Y_DELAY_4				

Registers to Control Pedestal and Gamma

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x34	PED_ON_1	[6]	0	0	**PED_ON_x** : Select to Pedestal ON/OFF (x = channel 1~4) **0** : Pedestal OFF **1** : Pedestal ON
	0x35	PED_ON_2				
	0x36	PED_ON_3				
	0x37	PED_ON_4				

Registers to Control Chrominance

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x38	CTI_GAIN_1	[7:0]	0x0A	0x0A	**CTI_GAIN_x[7:6]** **:** Adjust CTI Gain Delay **CTI_GAIN_x[4:0]** **:** Adjust gain level for CTI. (x = channel 1~4) **0x00** : No Gain **0x01 ~ 0x1F** : More larger gain
	0x39	CTI_GAIN_2				
	0x3A	CTI_GAIN_3				
	0x3B	CTI_GAIN_4				

- **Registers to Control Chrominance**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x3C	SATURATION_1	[7:0]	0x84	0x84	**SATURATION_x** : Color Gain Value (Adjustable up to x2) (x = channel 1~4) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x3D	SATURATION_2				
	0x3E	SATURATION_3				
	0x3F	SATURATION_4				
	0x40	HUE_1	[7:0]	0x00	0x00	**HUE_x** : Color HUE Control Value (360°/256 per HUE Value 1 unit) (x = channel 1~4) **00000000** : 0° **01000000** : 90° **10000000** : 180° **11111111** : 360°
	0x41	HUE_2				
	0x42	HUE_3				
	0x43	HUE_4				
	0x44	U_GAIN_1	[7:0]	0x00	0x00	**U_GAIN_x** : U Gain Value (Adjustable up to x2) (x = channel 1~4) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x45	U_GAIN_2				
	0x46	U_GAIN_3				
	0x47	U_GAIN_4				
	0x48	V_GAIN_1	[7:0]	0x00	0x00	**V_GAIN_x** : V Gain Value (Adjustable up to x2) (x = channel 1~4) **00000000** : x 0 **10000000** : x 1 **11000000** : x 1.5 **11111111** : x 2
	0x49	V_GAIN_2				
	0x4A	V_GAIN_3				
	0x4B	V_GAIN_4				
	0x4C	U_OFFSET_1	[7:0]	0x00	0x00	**U_OFFSET_x** : U offset value is adjustable up to ± 7. U offset consists of 2's complements. (x = channel 1~4) **0001** : + 1 **0111** : + 7 **1000** : - 8 **1111** : - 1
	0x4D	U_OFFSET_2				
	0x4E	U_OFFSET_3				
	0x4F	U_OFFSET_4				
	0x50	V_OFFSET_1	[7:0]	0x00	0x00	**V_OFFSET_x** : V offset value is adjustable up to ± 7. V offset consists of 2's complements. (x = channel 1~4) **0001** : + 1 **0111** : + 7 **1000** : - 8 **1111** : - 1
	0x51	V_OFFSET_2				
	0x52	V_OFFSET_3				
	0x53	V_OFFSET_4				

- **Registers to Control Field Polarity**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x54	FLD_INV_4	[7]	0xF	0x0	**FLD_INV_x** **:** Field Polarity Control (x = channel 1~4) **0** : not Inversion **1** : Inversion
		FLD_INV_3	[6]			
		FLD_INV_2	[5]			
		FLD_INV_1	[4]			

- **Registers to Insert No Video Information**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x54	NOVID_INF_IN_14	[3]	0x0	0x0	**NOVID_INF_IN _14** (x = channel 1~4) **:** It can include a NO-Video information at MSB of EAV and SAV. **0** : No information **1** : Put no-video information in EAV or SAV

- Registers to Control Channel **ID**

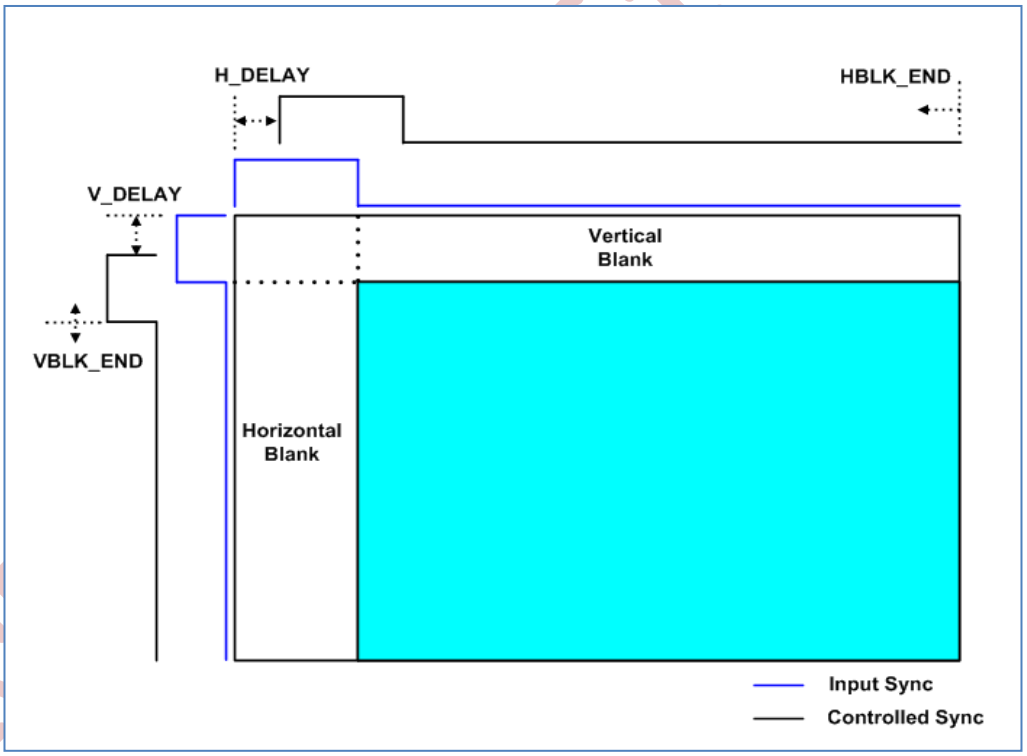
ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x54	CHID_TYPE_14	[2:0]	0x1	0x1	**CHID_TYPE_x** **:** It determines type of channel ID.(x = channel 1~4)
	0x55	CHID_VIN1	[3:0]	0x10	0x10	**CHID_VIN_x** **:** Register to put CHANNEL ID to distinguish channel. (0x0~0xF) (x = channel 1~4)
		CHID_VIN2	[7:4]			
	0x56	CHID_VIN3	[3:0]	0x10	0x10	
		CHID_VIN4	[7:4]			

- Registers to Control Video Output **Timing**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x58	H_DELAY_1	[7:0]	0x8B	0x80	**H_DELAY_x** **:** Register to determine the Horizontal start position of output image to Hsync extracted in analog input signal. (x = channel 1~4)
	0x59	H_DELAY_2				
	0x5A	H_DELAY_3				
	0x5B	H_DELAY_4				
	0x5C	V_DELAY_1	[7:0]	0x9E	0x9E	**V_DELAY_x[7:6]** **:** Select to vblk_str_fld (x = channel 1~4) **00 : evenfld 01 : !evenfld 10 : 0 11 : 1** **V_DELAY_x[5]** **:** V_DELAY_x[4:0] Control Enable (x = channel 1~4) **V_DELAY_x[4:0] (When V_DELAY_x[5] = 1)** **:** Register to determine the Vertical start position of output image to Vsync extracted in analog input signal. (x = channel 1~4)
	0x5D	V_DELAY_2				
	0x5E	V_DELAY_3				
	0x5F	V_DELAY_4				

- **Registers to Control Video Output Timing**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x60	HBLK_END_1	[7:0]	0x00	0x00	**HBLK_END_x** **:** Register to control Width of Horizontal Blanking, If user increments or decrements the value of this register, then the Active region is changed. (x = channel 1~4)
	0x61	HBLK_END_2				
	0x62	HBLK_END_3				
	0x63	HBLK_END_4				
	0x64	VBLK_END_1	[7:0]	0xC0 SD 0x28	0xC0 SD 0x2D	**VBLK_END_x[7:6]** **:** Select to vblk_end_fld (x = channel 1~4) **00 : evenfld 01 : !evenfld 10 : 0 11 : 1** **VBLK_END_x[5]** **:** VBLK_END_x[4:0] Control Enable (x = channel 1~4) **VBLK_END_x[4:0] (When VBLK_END_x[5] = 1)** **:** Register to control Width of Vertical Blanking. If user increments or decrements the value of this register, then the Active region is changed. (x = channel 1~4)
	0x65	VBLK_END_2				
	0x66	VBLK_END_3				
	0x67	VBLK_END_4				



Registers to Control Video Output Timing

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x68	H_CROP_S_1	[7:0]	0x00	0x00	**H_CROP_S_x** : Adjust the horizontal crop start point. (x = channel 1~4)
	0x69	H_CROP_S_2				
	0x6A	H_CROP_S_3				
	0x6B	H_CROP_S_4				
	0x6C	H_CROP_E_1	[7:0]	0x00	0x00	**H_CROP_E_x** : Adjust the horizontal crop end point. (x = channel 1~4)
	0x6D	H_CROP_E_2				
	0x6E	H_CROP_E_3				
	0x6F	H_CROP_E_4				
	0x70	V_CROP_S_1	[7:0]	0x00	0x00	**V_CROP_S_x** : Adjust the vertical crop start point. (x = channel 1~4)
	0x71	V_CROP_S_2				
	0x72	V_CROP_S_3				
	0x73	V_CROP_S_4				
	0x74	V_CROP_E_1	[7:0]	0x00	0x00	**V_CROP_E_x** : Adjust the vertical crop end point. (x = channel 1~4)
	0x75	V_CROP_E_2				
	0x76	V_CROP_E_3				
	0x77	V_CROP_E_4				

Registers to Control Back Ground Color

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x78	BGDCOL_1	[3:0]	0x88	0x88	**BGDCOL_x** **:** When No-Video, BackGround Color is used. (x = channel 1~4) **0000** : Blue **0001** : White (75%) **0010** : Yellow **0011** : Cyan **0100** : Green **0101** : Magenta **0110** : Red **0111** : Blue **1000** : Black **1001** : Gray **1010** : Red (NEXTCHIP*) **1011** : Yellow (NEXTCHIP*) **1100** : Magenta (NEXTCHIP*) **1101** : Green (NEXTCHIP*) **1110** : Blue (NEXTCHIP*) **1111** : Cyan (NEXTCHIP*) *** These color information is exactly same as controllers provided by NEXTCHIP**
		BGDCOL_2	[7:4]			
	0x79	BGDCOL_3	[3:0]			
		BGDCOL_4	[7:4]			

- **Registers to Control Data Out Mode**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x7A	DATA_OUT_MODE_1	[3:0]	0x11	0x11	**DATA_OUT_MODE_x** **:** It limits a level of output data, can change signals of Cb and Cr each. (x = channel 1~4) **0000** : Y(016~235), Cb(016~240), Cr(016~240) **0001** : Y(001~254), Cb(001~254), Cr(001~254) **0010** : Y(000~255), Cb(000~255), Cr(000~255) **0011** : Cb / Cr Change, 016~235 **0100** : Cb / Cr Change, 001~254 **0101** : Cb / Cr Kill, 016~235 **0110** : Cb / Cr Kill, 001~254 **Others** : Background color output
		DATA_OUT_MODE_2	[7:4]			
	0x7B	DATA_OUT_MODE_3	[3:0]			
		DATA_OUT_MODE_4	[7:4]			

6.2.2 Enable Registers

- **Registers For Each Channel Control**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x80	EACH_REG_SET	[3:0]	0xF	0xF	**DEC_REG_EACH** **:** For each control CH1~CH4 register. **0x0 :** same control **0xF :** each control

- **Registers to Select AHD Mode**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x81	AHD_MD_1	[3:0]	0x2	0x3	**AHD_MD_x** **:** AHD Mode Selection. **0:** SD Mode **3:** 1080 25P MODE **5:** 720 50P MODE **7:** 720 25P MODE **B:** 720 25P_EX MODE **2:** 1080 30P MODE **4:** 720 60P MODE **6:** 720 30P MODE **A:** 720 30P_EX MODE **Etc.:** Don't use
	0x82	AHD_MD_2				
	0x83	AHD_MD_3				
	0x84	AHD_MD_4				
	0x81	SD_MD_1	[7:4]	0x0	0x0	**SD_MD** **:** SD Mode Selection. **0:** SD NTSC Mode **A:** SD_EX NTSC MODE **C:** SD_2EX NTSC MODE **1:** SD PAL MODE **B:** SD_EX PAL MODE **D:** SD_2EX PAL MODE **Etc.:** Don't use
	0x82	SD_MD_2				
	0x83	SD_MD_3				
	0x84	SD_MD_4				

- **Registers to Control H_DELAY**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x8E	H_DLY_MSB_1	[7:4]	0x0	0x0	**HDLY_MSBS_0x** **:** MSB[3:0] Register of H_DELAY Register (Bank0 0x58~5B)
	0x8F	H_DLY_MSB_2				
	0x90	H_DLY_MSB_3				
	0x91	H_DLY_MSB_4				

- **Registers to Control Horizontal ZOOM**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0x93	HZOOM_ON_1	[0]	0x0	0x0	**HZOOM_ON_x** (x = channel number) **:** This Register can be turned on or off Horizontal ZOOM. (* H_ZOOM can use only in SD MODE.) **0:** ZOOM OFF **1:** ZOOM ON
	0x94	HZOOM_ON_2				
	0x95	HZOOM_ON_3				
	0x96	HZOOM_ON_4				
	0x98	ZOOM_DTO_1	[3:0]	0x0	0x0	**ZOOM_DTO _x** (x = channel 1~4) **:** H_ZOOM Step Control.
	0x99	ZOOM_DTO_2	[3:0]			
	0x9A	ZOOM_DTO_3	[3:0]			
	0x9B	ZOOM_DTO_4	[3:0]			

- **Registers to Control Y/C DELAY**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xA0	DF_YDELAY_4	[3:0]	0x00	0x00	**DF_YDELAY_x** (x = channel 1~4) : Y(Luminance) delay control in the domain of 27MHz can be controlled between 0x0 ~ 0xF.
	0xA1	DF_YDELAY_3				
	0xA2	DF_YDELAY_2				
	0xA3	DF_YDELAY_1				
	0xA0	DF_CDELAY_4	[7:4]	0x00	0x00	**DF_CDELAY_x** (x = channel 1~4) : C(Chrominance) delay control in the domain of 27MHz can be controlled between 0x0 ~ 0xF.
	0xA1	DF_CDELAY_3				
	0xA2	DF_CDELAY_2				
	0xA3	DF_CDELAY_1				

6.2.3 State Registers

- **Registers to Status Registers (Read Only)**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xA8	NOVID_01	[0]	Read	Read	**NOVID_0x** **:** Each Channel Video Decoder No Video detection Status. (x = Channel number) **0** : On Video **1** : No Video
		NOVID_02	[1]			
		NOVID_03	[2]			
		NOVID_04	[3]			
	0xA9	MOTION_01	[0]	Read	Read	**MOTION_0x** **:** Each Channel Motion detection Status (x = Channel number) **0** : No MOTION **1** : On MOTION
		MOTION_02	[1]			
		MOTION_03	[2]			
		MOTION_04	[3]			

- **Registers to Status Registers (Read Only)**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xAC	MUTE _01	[0]	Read	Read	**MUTE_0x** **:** Each Channel MUTE detection Status (x = Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTE _02	[1]			
		MUTE_03	[2]			
		MUTE_04	[3]			
		MUTE_05	[4]			
		MUTE_06	[5]			
		MUTE_07	[6]			
		MUTE_08	[7]			
	0xAD	MUTE_09	[0]	Read	Read	
		MUTE_10	[1]			
		MUTE_11	[2]			
		MUTE_12	[3]			
		MUTE_13	[4]			
		MUTE_14	[5]			
		MUTE_15	[6]			
		MUTE_16	[7]			
	0xAE	MUTEMIC_01	[0]	Read	Read	**MUTEMIC_01~02** : Each Internal and External Mic Channel MUTE detection Status **0** : On Audio **1** : No Audio (MUTE)
		MUTEMIC_02	[1]			
	0xAF	COAX_RX_DONE_1	[0]	Read	Read	**COAX_RX_DONE_x** **:** COAXIAL_RX_Detecting Status (x = channel number) **0** : No Detecting **1** : COAXIAL_RX_Detecting
		COAX_RX_DONE_2	[1]			
		COAX_RX_DONE_3	[2]			
		COAX_RX_DONE_4	[3]			

● **Registers to Interrupt clear for Status Registers**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xB0	NOVID_01B	[0]	Read	Read	**NOVID_0xB** : Each Channel Video Decoder No Video detection Status with HOLD option (x = Channel number) **0** : On Video **1** : No Video
		NOVID_02B	[1]			
		NOVID_03B	[2]			
		NOVID_04B	[3]			
	0xB1	MOTION_01B	[0]	Read	Read	**MOTION_0xB** : Each Channel Motion detection Status with HOLD option (x = Channel number) **0** : No MOTION **1** : On MOTION
		MOTION_02B	[1]			
		MOTION_03B	[2]			
		MOTION_04B	[3]			

● **Registers to Interrupt clear for Status Registers**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xB4	MUTE_01B	[0]	Read	Read	**MUTE_0xB** : Each Channel MUTE detection Status with HOLD option (x = Channel number) **0** : On Audio **1** : No Audio (MUTE)
		MUTE_02B	[1]			
		MUTE_03B	[2]			
		MUTE_04B	[3]			
		MUTE_05B	[4]			
		MUTE_06B	[5]			
		MUTE_07B	[6]			
		MUTE_08B	[7]			
	0xB5	MUTE_09B	[0]	Read	Read	
		MUTE_10B	[1]			
		MUTE_11B	[2]			
		MUTE_12B	[3]			
		MUTE_13B	[4]			
		MUTE_14B	[5]			
		MUTE_15B	[6]			
		MUTE_16B	[7]			
	0xB6	MUTEMIC_01B	[0]	Read	Read	**MUTEMIC_01~02B** : Each Internal and External Mic 2 Channel MUTE detection Status **0** : On Audio **1** : No Audio (MUTE)
		MUTEMIC_02B	[1]			

● **Registers to Interrupt clear for Status Registers**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xB7	COAX_RX_DONE_1B	[0]	Read	Read	**COAX_RX_DONE_x** : COAXIAL_RX_Detecting Checking Status (x = channel number) **0** : No Detecting **1** : COAXIAL_RX_Detecting
		COAX_RX_DONE_2B	[1]			
		COAX_RX_DONE_3B	[2]			
		COAX_RX_DONE_4B	[3]			

- **Registers to Interrupt clear for Status Registers**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xB8	RD_STATE_CLR	[7]	0x90	0x90	**RD_STATE_CLR** **:** Interrupt clear condition selection **0 :** Interrupt clear when BANK0, 0xC0~0xC6 Addr Register Read **1 :** Interrupt clear when BANK0, 0xB8~0xBE / 0xC0~0xC6 Addr Register Read
		STATE_HOLD	[4]			**STATE_HOLD** **:** Interrupt Hold condition selection **0 :** No Hold Option, State is Real Time update. **1 :** Hold Option operation. State is Hold until cleared

- **Registers to Control IRQ**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xB9	IRQ_MSB	[4]	0x00	0x00	**IRQ_MSB** **:** Control output data of IRQ pin **0 :** 1 item output for MPP signal **1 :** 2~5 item OR output for MPP signal
		IRQ_INV	[3]			**IRQ_INV** **:** IRQ pin output signal inversion **0 :** Not Inversion **1 :** Inversion
		IRQ_SEL	[2:0]			**IRQ_SEL** **:** Select IRQ pin output signals selection When IRQ_MSB(BANK1,0xB9[4]) = 0, **0 : 0 (Zero)** **1 :** interrupt request by the No video detection **2 :** interrupt request by the Mute detection **3 :** interrupt request by the Motion detection **4 :** interrupt request by the Black detection **5 :** interrupt request by the White detection **6 :** ALINKO **7 :** BNCO When IRQ_MSB(BANK1,0xB9[4]) = 1, **0 :** Novid | Motion interrupt request **1 :** Novid | Black interrupt request **2 :** Novid | White interrupt request **3 :** Black | White interrupt request **4 :** Black | Motion interrupt request **5 :** White | Motion interrupt request **6 :** Novid | Motion | Black interrupt request **7 :** Black | White | Motion interrupt request

Registers to Show Locking Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xE0	AGC_LOCK_04	[3]	Read	Read	**AGC_LOCK_0x** **:** Video AGC Locking Status (x = channel number) **0** : No Locking **1** : Locking
		AGC_LOCK_03	[2]			
		AGC_LOCK_02	[1]			
		AGC_LOCK_01	[0]			
	0xE1	CMP_LOCK_04	[3]	Read	Read	**CMP_LOCK_0x** **:** Video CLAMP Locking status (x = channel number) **0** : No Locking **1** : Locking
		CMP_LOCK_03	[2]			
		CMP_LOCK_02	[1]			
		CMP_LOCK_01	[0]			
	0xE2	H_LOCK_04	[3]	Read	Read	**H_LOCK_0x** **:** Video Horizontal Locking status (x = channel number) **0** : No Locking **1** : Locking
		H_LOCK_03	[2]			
		H_LOCK_02	[1]			
		H_LOCK_01	[0]			

Registers to Show Chip Status (Read Only)

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xE7	BW_04	[3]	Read	Read	**BW_0x** **:** Black / White Detection status (x = channel number) **0** : Color **1** : B/W
		BW_03	[2]			
		BW_02	[1]			
		BW_01	[0]			

- **Registers to read the FSC Status (Read Only)**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xE8	FSC_CHG_DONE_01	[3]	Read	Read	**FSC_CHG_DONE _x** **:** A status which FSC changed done or not (x = channel number) **0 :** not changed **1 :** changed
	0xE9	FSC_CHG_DONE_02				
	0xEA	FSC_CHG_DONE_03				
	0xEB	FSC_CHG_DONE_04				
	0xE8	CKILL_01	[2]	Read	Read	**CKILL _x** **:** color kill status (x = channel number) **0 :** Color On **1 :** Color Off
	0xE9	CKILL_02				
	0xEA	CKILL_03				
	0xEB	CKILL_04				
	0xE8	FSC_LOCK_DONE_01	[1]	Read	Read	**FSC_LOCK_DONE_x** : FSC LOCK Detection Status (x = channel number)
	0xE9	FSC_LOCK_DONE_02				
	0xEA	FSC_LOCK_DONE_03				
	0xEB	FSC_LOCK_DONE_04				
	0xE8	NOVIDEO_01	[0]	Read	Read	**NOVIDEO_x** : NOVIDEO Status (x=channel number)
	0xE9	NOVIDEO_02				
	0xEA	NOVIDEO_03				
	0xEB	NOVIDEO_04				

- **Registers to Show Chip Status (Read Only)**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
0	0xF4	DEV_ID	[7:0]	Read	Read	**DEV_ID** **:** It shows Device ID (NVP6134 = 0x91)
	0xF5	REV_ID	[7:0]	Read	Read	**REV_ID** **:** It shows Revision ID (0x01)

6.2.4 AUDIO Registers

- **Registers to Control Audio AFE and DFE**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x00	PD_AU_AFE	[7]	0x02	0x02	**PD_AU_AFE** **:** Audio AFE LIVE CH1~CH4 and MIC1 Power Down Mode selection 0 : Operation 1 : Power Down
		PD_AU_DAC	[6]			**PD_AU_DAC** **:** Audio DAC Power Down Mode selection 0 : Operation 1 : Power Down
		RM_PB_PIN	[3]			**RM_PB_PIN** **:** Selection of clock and sync for ADATA_REC, ADATA_SP pin 0 : use ACLK_REC and ASYNC_REC as clock and sync for ADATA_REC, ADATA_SP pin 1 : use ACLK_PB and ASYNC_PB as clock and sync for ADATA_REC, ADATA_SP pin
		PB_RM_PIN	[2]			**PB_RM_PIN** **:** Selection of clock and sync for ADATA_PB pin 0 : use ACLK_PB and ASYNC_PB as clock and sync for ADATA_PB, 1 : use ACLK_REC and ASYNC_REC as clock and sync for ADATA_PB,
		FILTER_ON	[1]			**FILTER_ON** **:** Set ADC sampling rate 0 : Non-oversample (16KHz) 1 : Oversample (64KHz)
		EN_32K_MODE	[0]			**EN_32K_MODE** **:** Operate whole audio system as 32K mode 0 : 16K Mode 1 : 32K Mode

- **Registers to Control Audio Input Gain**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x01	AIGAIN_01	[7:0]	0x08	0x08	**AIGAIN_x / MIGAIN_x** **:** The gain of analog audio input AIN1-8 and MICIN1 **0000** : mute **0001** : 0.125 **0010** : 0.25 **0011** : 0.375 **0100** : 0.5 **0101** : 0.625 **0110** : 0.75 **0111** : 0.875 **1000** : 1.0 **1001** : 1.125 **1010** : 1.25 **1011** : 1.375 **1100** : 1.5 **1101** : 1.625 **1110** : 1.75 **1111** : 1.875 **10000** : 2.0 **10001** : 2.125 **10000 ~ 11111111 :** step by about 0.125
	0x02	AIGAIN_02	[7:0]			
	0x03	AIGAIN_03	[7:0]			
	0x04	AIGAIN_04	[7:0]			
	0x40	AIGAIN_05	[7:0]			
	0x41	AIGAIN_06	[7:0]			
	0x42	AIGAIN_07	[7:0]			
	0x43	AIGAIN_08	[7:0]			
	0x05	MIGAIN_01	[3:0]			

- **Registers to Audio Interface**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x06	CAS_PB	[7]	0x1B	0x1B	**CAS_PB** : The Usage of Playback Data when Cascade Mode **0** : use multiple playback data, received through all stage **1** : use single playback data, received through last stage
		TRANS_MODE	[6]			**TRANS_MODE** : Control the phase between transferred clock and cascade data **0** : Same phase **1** : Inverted phase
		CAS_PIN	[4]			**CAS_PIN** : Control the usage of ADATA_CASI and ADATA_CASO as cascade transmitting **0** : Don't Use **1** : Use
		CASCADE_MODE	[3]			**CASCADE_MODE** : Set the chip position when it is cascaded. **0** : ACLK/ASYNC/ADATA Use **1** : ALINKI/ALINKO Use
		CHIP_STAGE	[1:0]			**CHIP_STAGE** : Selection of chip state for cascade **0** : middle stage **1** : last stage **2** : first stage **3** : single chip operation
	0x07	RM_MASTER	[7]	0xC8	0xC8	**RM_MASTER** : Selection of master & slave mode of ACLK_REC and ASYNC_REC **0** : Slave mode operation **1** : Master mode operation
		RM_CLK	[6]			**RM_CLK** : Set the relationship between audio signal outputted to ADATA_REC and clock outputted to ACLK_REC **0** : inverted clock **1** : non-inverted clock
		RM_BITRATE	[5:4]			**RM_BITRATE** : Set the bit rate of audio signal outputted to ADATA_REC **0** : 256fs **1** : **384**fs **2** : 320fs **3** : Don't Use
		RM_SAMRATE	[3]			**RM_SAMRATE** : Set the sampling rate of data outputted to ADATA_REC **0** : 8KHz **1** : 16KHz
		RM_BITWID	[2]			**RM_BITWID** : Set the bit width of data outputted to ADATA_REC **0** : 16bits **1** : 8bits
		RM_SSP	[1]			**RM_SSP** : Selection of DSP mode and SSP mode for ADATA_REC pin, when ASYNC_REC is DSP mode. **0** : DSP mode **1** : SSP mode
		RM_SYNC	[0]			**RM_SYNC** : Set the sync's mode inputted/outputted to ASYNC_REC. **0** : I2S mode **1** : DSP mode

Registers to Control Audio interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x08	RM_BIT_SWAP	[7]	0x03	0x03	**RM_BIT_SWAP** **:** Set the bit sequence of Audio Data for ADATA_REC **0** : MSB first **1** : LSB first
		RM_LAW_SEL	[6]			**RM_LAW_SEL** **:** Define the G.711 data format outputted to ADATA_REC **0** : u-law **1** : a-law
		RM_FORMAT	[5:4]			**RM_FORMAT** **:** Define the data format outputted to ADATA_REC **0** : linear PCM **1** : Unsigned linear PCM **2** : G.711 format **3** : Don't Use
		R_ADATSP	[2]			**R_ADATSP** **:** Selection of output data for ADATA_SP **0** : Speaker data **1** : Record data
		R_MULTCH	[1:0]			**R_MULTCH** **:** Selection of number of Channel for ADATA_REC **0** : 2ch **1** : 4ch **2** : 8ch **3** : 16ch

Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x09	R_SEQ_01[4]	[0]	0x0	0x0	**R_SEQ** **:** Sequence of Audio Data for ADATA_REC **00000** : channel 1 data **00001** : channel 2 data **00010** : channel 3 data **00011** : channel 4 data **00100** : channel 5 data **00101** : channel 6 data **00110** : channel 7 data **00111** : channel 8 data **01000** : channel 9 data **01001** : channel 10 data **01010** : channel 11 data **01011** : channel 12 data **01100** : channel 13 data **01101** : channel 14 data **01110** : channel 15 data **01111** : channel 16 data **10000** : Mic input 1 **10001** : Mic input 2
		R_SEQ_02[4]	[1]	0x0	0x0	
		R_SEQ_03[4]	[2]	0x0	0x0	
		R_SEQ_04[4]	[3]	0x0	0x0	
		R_SEQ_05[4]	[4]	0x0	0x0	
		R_SEQ_06[4]	[5]	0x0	0x0	
		R_SEQ_07[4]	[6]	0x0	0x0	
		R_SEQ_08[4]	[7]	0x0	0x0	
	0x0A	R_SEQ_01[3:0]	[3:0]	0x10	0x10	
		R_SEQ_02[3:0]	[7:4]			
	0x0B	R_SEQ_03[3:0]	[3:0]	0x32	0x32	
		R_SEQ_04[3:0]	[7:4]			
	0x0C	R_SEQ_05[3:0]	[3:0]	0x54	0x54	
		R_SEQ_06[3:0]	[7:4]			
	0x0D	R_SEQ_07[3:0]	[3:0]	0x76	0x76	
		R_SEQ_08[3:0]	[7:4]			

Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x0E	R_SEQ_09[4]	[0]	0x0	0x0	**R_SEQ_xx / MIC_SEQ_0x.** (x = channel number) **:** Sequence of Audio Data for ADATA_REC **00000** : channel 1 data **00001** : channel 2 data **00010** : channel 3 data **00011** : channel 4 data **00100** : channel 5 data **00101** : channel 6 data **00110** : channel 7 data **00111** : channel 8 data **01000** : channel 9 data **01001** : channel 10 data **01010** : channel 11 data **01011** : channel 12 data **01100** : channel 13 data **01101** : channel 14 data **01110** : channel 15 data **01111** : channel 16 data **10000** : Mic input 1 **10001** : Mic input 2
		R_SEQ_10[4]	[1]	0x0	0x0	
		R_SEQ_11[4]	[2]	0x0	0x0	
		R_SEQ_12[4]	[3]	0x0	0x0	
		R_SEQ_13[4]	[4]	0x0	0x0	
		R_SEQ_14[4]	[5]	0x0	0x0	
		R_SEQ_15[4]	[6]	0x0	0x0	
		R_SEQ_16[4]	[7]	0x0	0x0	
	0x0F	R_SEQ_09[3:0]	[3:0]	0x98	0x98	
		R_SEQ_10[3:0]	[7:4]			
	0x10	R_SEQ_11[3:0]	[3:0]	0xBA	0xBA	
		R_SEQ_12[3:0]	[7:4]			
	0x11	R_SEQ_13[3:0]	[3:0]	0xDC	0xDC	
		R_SEQ_14[3:0]	[7:4]			
	0x12	R_SEQ_15[3:0]	[3:0]	0xFE	0xFE	
		R_SEQ_16[3:0]	[7:4]			
	0x3C	MIC_SEQ_01	[4:0]	0x10	0x10	
	0x3D	MIC_SEQ_02	[4:0]	0x11	0x11	

Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x13	PB_MASTER	[7]	0x08	0x08	**PB_MASTER** **:** Selection of master & slave mode of ACLK_PB and ASYNC_PB **0** : Slave mode **1** : Master mode
		PB_CLK	[6]			**PB_CLK** **:** Set the relationship between audio signal outputted to ADATA_PB and clock outputted to ACLK_PB **0** : inverted clock **1** : non-inverted clock
		PB_BITRATE	[5:4]			**PB_BITRATE** **:** Set the bit rate of audio signal outputted to ADATA_PB **0** : 256fs **1** : 384fs **2** : 320fs
		PB_SAMRATE	[3]			**PB_SAMRATE** **:** Set the sampling rate of data outputted to ADATA_PB **0** : 8KHz **1** : 16KHz
		PB_BITWID	[2]			**PB_BITWID** **:** Set the bit width of data outputted to ADATA_PB **0** : 16bits **1** : 8bits
		PB_SSP	[1]			**PB_SSP** **:** Set the position of data and sync signals inputted to ADATA_PB, when ASYNC_PB is DSP mode. **0** : DSP mode **1** : SSP mode
		PB_SYNC	[0]			**PB_SYNC** **:** Set the sync's mode inputted/outputted to ASYNC_PB. **0** : I2S mode **1** : DSP mode

Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x14	PB_BIT_SWAP	[7]	0x00	0x00	**PB_BIT_SWAP** **:** Set the bit sequence of Audio Data for ADATA_PB **0** : MSB first **1** : LSB first
		PB_SEL	[4:0]			**PB_SEL** **:** select the audio input channel for playback input **00** : channel 01 **01** : channel 02 **02** : channel 03 **03** : channel 04 **04** : channel 05 **05** : channel 06 **06** : channel 07 **07** : channel 08 **08** : channel 09 **09** : channel 10 **0A** : channel 11 **0B** : channel 12 **0C** : channel 13 **0D** : channel 14 **0E** : channel 15 **0F** : channel 16 **10** : Mic input 1 **11** : Mic input 2

Registers to Control Audio Interface

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x15	PB_FORMAT	[7:6]	0x00	0x00	**PB_FORMAT** **:** Define the data format inputted to ADATA_PB **0** : linear PCM **1** : Unsigned linear PCM **2** : G.711 format **3** : Don't Use
		PB_LAW_SEL	[3]			**PB_LAW_SEL** **:** Define the G.711 data format inputted to ADATA_PB **0** : u-law **1** : a-law

Registers to Control Audio Mixing Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x16	MIX_RATIO_01	[3:0]	0x88	0x88	**MIX_RATIO_x** **:** Set the mixing gain for AIN1-15. (x = channel number) **0** : mute **1** : 0.25 **2** : 0.31 **3** : 0.38 **4** : 0.5 **5** : 0.63 **6** : 0.75 **7** : 0.88 **8** : 1.0 **9** : 1.25 **10** : 1.5 **11** : 1.75 **12** : 2.0 **13** : 2.25 **14** : 2.5 **15** : 2.75
		MIX_RATIO_02	[7:4]			
	0x17	MIX_RATIO_03	[3:0]			
		MIX_RATIO_04	[7:4]			
	0x18	MIX_RATIO_05	[3:0]			
		MIX_RATIO_06	[7:4]			
	0x19	MIX_RATIO_07	[3:0]			
		MIX_RATIO_08	[7:4]			
	0x1A	MIX_RATIO_09	[3:0]			
		MIX_RATIO_10	[7:4]			
	0x1B	MIX_RATIO_11	[3:0]			
		MIX_RATIO_12	[7:4]			
	0x1C	MIX_RATIO_13	[3:0]			
		MIX_RATIO_14	[7:4]			
	0x1D	MIX_RATIO_15	[3:0]			
		MIX_RATIO_16	[7:4]			

Registers to Control Audio Mixing Gain

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x1E	MIX_RATIO_M1	[3:0]	0x88	0x88	**MIX_RATIO_Mx/ MIX_RATIO_Px** **:** Set the mixing gain for MICIN1~2 / PBIN1~4. (x = channel number) **0** : mute **1** : 0.25 **2** : 0.31 **3** : 0.38 **4** : 0.5 **5** : 0.63 **6** : 0.75 **7** : 0.88 **8** : 1.0 **9** : 1.25 **10** : 1.5 **11** : 1.75 **12** : 2.0 **13** : 2.25 **14** : 2.5 **15** : 2.75
		MIX_RATIO_M2	[7:4]			
	0x20	MIX_RATIO_P1	[3:0]			
		MIX_RATIO_P2	[7:4]			
	0x21	MIX_RATIO_P3	[3:0]			
		MIX_RATIO_P4	[7:4]			
	0x22	AOGAIN	[7:0]	0x08	0x08	**AOGAIN** **:** The gain of analog audio output **0000** : mute **0001** : 0.125 **0010** : 0.25 **0011** : 0.375 **0100** : 0.5 **0101** : 0.625 **0110** : 0.75 **0111** : 0.875 **1000** : 1.0 **1001** : 1.125 **1010** : 1.25 **1011** : 1.375 **1100** : 1.5 **1101** : 1.625 **1110** : 1.75 **1111** : 1.875 **10000 ~ 11111111 :** step by about 0.125

Registers to Control Audio Mixing Output Mode

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x23	MIX_DERATIO	[5]	0x19	0x19	**MIX_DERATIO** **:** Selection of the mixing gain mode **0 :** Apply the mixing gain for MIX_RATIO_01-P4 (BANK1,0x16~0x21 Addr) separately **1 :** Apply all mixing gain as the same gain (x1).
		MIX_OUTSEL	[4:0]			**MIX_OUTSEL** **:** Select the audio output for analog mixing out. **00** : Channel 1 **0E** : Channel 15 **01** : Channel 2 **0F** : Channel 16 **02** : Channel 3 **10** : playback audio **03** : Channel 4 (first stage playback audio) **04** : Channel 5 **11** : second playback audio **05** : Channel 6 (middle stage playback audio) **06** : Channel 7 **12** : third playback audio **07** : Channel 8 (middle stage playback audio) **08** : Channel 9 **13** : fourth playback audio **09** : Channel 10 (last stage playback audio) **0A** : Channel 11 **14** : Mic input 1 **0B** : Channel 12 **15** : Mic input 2 **0C** : Channel 13 **18** : Mixed audio **0D** : Channel 14 **Others** : No audio output

Registers to Select Audio Output for ADATA_SP PIN

AD DRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x24	L_CH_OUTSEL	[4:0]	0x19	0x19	**L_CH_OUTSEL / R_CH_OUTSEL** **:** Select Left/Right channel of the audio output for ADATA_SP pin **00** : Channel 1 **01** : Channel 2 **02** : Channel 3 **03** : Channel 4 **04** : Channel 5 **05** : Channel 6 **06** : Channel 7 **07** : Channel 8 **08** : Channel 9 **09** : Channel 10 **0A** : Channel 11 **0B** : Channel 12 **0C** : Channel 13 **0D** : Channel 14 **0E** : Channel 15 **0F** : Channel 16 **10** : playback audio (first stage playback audio) **11** : second playback audio (middle stage playback audio) **12** : third playback audio (middle stage playback audio) **13** : fourth playback audio (last stage playback audio) **14** : Mic input 1 **15** : Mic input 2 **18** : Mixed audio **Others** : No audio output
	0x25	R_CH_OUTSEL		0x19	0x19	

Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x26	MIX_MUTE_01	[0]	0x00	0x00	**MIX_MUTE_x** **:** During mixing, selected channels are muted (x = channel value) **0** : mixing data output **1** : mute for selected channel
		MIX_MUTE_02	[1]			
		MIX_MUTE_03	[2]			
		MIX_MUTE_04	[3]			
		MIX_MUTE_05	[4]			
		MIX_MUTE_06	[5]			
		MIX_MUTE_07	[6]			
		MIX_MUTE_08	[7]			
	0x27	MIX_MUTE_09	[0]			
		MIX_MUTE_10	[1]			
		MIX_MUTE_11	[2]			
		MIX_MUTE_12	[3]			
		MIX_MUTE_13	[4]			
		MIX_MUTE_14	[5]			
		MIX_MUTE_15	[6]			
		MIX_MUTE_16	[7]			
	0x28	MIX_MUTE_P1	[0]			
		MIX_MUTE_P2	[1]			
		MIX_MUTE_P3	[2]			
		MIX_MUTE_P4	[3]			
		MIX_MUTE_M1	[4]			
		MIX_MUTE_M2	[5]			

Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x29	AUTO_MUTE	[7]	0x88	0x88	**AUTO MUTE Detection** **0** : Absolute amplitude detection mode **1** : Differential amplitude detection mode
		ADET_FILT	[2:0]			**ADET_FILT** **:** Set the time to decide the existence of audio signals. **0** : 16sec **1** : 15sec **2** : 9sec **3** : 5sec **4** : 3sec **5** : 1sec **6** : 0.6sec **7** : 0.5sec

Registers to Control Audio Detection

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x2A	ADET_01	[0]	0xFF	0xFF	**ADET_0x / ADET_Mx** **:** Enable bit audio signal existence checking function for AIN1-8 and MICIN1. (x = channel 1~8) **0** : Don't use this function **1** : Use this function
		ADET_02	[1]			
		ADET_03	[2]			
		ADET_04	[3]			
		ADET_05	[4]			
		ADET_06	[5]			
		ADET_07	[6]			
		ADET_08	[7]			
	0x2B	ADET_M1	[6]	0x40	0x40	

Registers to Control Audio CLK

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x38	AUD_SW_RST	[4]	0x08	0x08	**AUD_SW_RST** **:** Software Reset **0** : Normal Operation **1** : Reset

Registers to Control Audio DAC GAIN

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x3A	A_DAC_GAIN	[3:0]	0x03	0x03	**A_DAC_GAIN** **:** Digital Input to Analog Output Gain Control Analog output is 2Vpp when gain setting is 0dB and digital input is full scale **0 :** -3dB **8 :** 5dB **1 :** -2dB **9 :** 6dB **2 :** -1dB **10 :** 7dB **3 :** 0dB **11 :** 8dB **4 :** 1dB **12 :** 9dB **5 :** 2dB **13 :** 10dB **6 :** 3dB **14 :** 11dB **7 :** 4dB **15 :** 12dB

- **Registers to Control Audio AFE**

<table>
<tr><th colspan="2">ADDRESS</th><th rowspan="2">REGISTER NAME</th><th rowspan="2">BITS</th><th colspan="2">VALUE</th><th rowspan="2">DESCRIPTION</th></tr>
<tr><th>Bank</th><th>Addr</th><th>30P</th><th>25P</th></tr>
<tr><td>1</td><td>0x3B</td><td>A_GAIN_SEL(AFE)</td><td>[7:4]</td><td>0x3</td><td>0x3</td><td>
A_GAIN_SEL(AUDIO AFE)
: Analog Gain Control for AIN 1 ~ 4, MicIN1
<table>
<tr><th>A_GAIN_SEL<3:0></th><th>Gain</th><th>Low</th><th>Mid</th><th>High</th><th>Input Vpp</th></tr>
<tr><td>0000</td><td>0.25x</td><td>-0.60</td><td>1.60</td><td>3.60</td><td>4.00</td></tr>
<tr><td>0001</td><td>0.50x</td><td>0.60</td><td>1.60</td><td>2.60</td><td>2.00</td></tr>
<tr><td>0010</td><td>0.75x</td><td>0.93</td><td>1.60</td><td>2.27</td><td>1.33</td></tr>
<tr><td>0011</td><td>1.00x</td><td>1.10</td><td>1.60</td><td>2.10</td><td>1.00</td></tr>
<tr><td>0100</td><td>1.25x</td><td></td><td>1.60</td><td></td><td>0.80</td></tr>
<tr><td>0101</td><td>1.50x</td><td></td><td>1.60</td><td></td><td>0.67</td></tr>
<tr><td>0110</td><td>1.75x</td><td></td><td>1.60</td><td></td><td>0.57</td></tr>
<tr><td>0111</td><td>2.00x</td><td>1.35</td><td>1.60</td><td>1.85</td><td>0.50</td></tr>
<tr><td>1000</td><td>2.25x</td><td></td><td>1.60</td><td></td><td>0.44</td></tr>
<tr><td>1001</td><td>2.50x</td><td></td><td>1.60</td><td></td><td>0.40</td></tr>
<tr><td>1010</td><td>2.75x</td><td></td><td>1.60</td><td></td><td>0.36</td></tr>
<tr><td>1011</td><td>3.00x</td><td>1.54</td><td>1.60</td><td>1.77</td><td>0.33</td></tr>
<tr><td>1100</td><td>3.25x</td><td></td><td>1.60</td><td></td><td>0.31</td></tr>
<tr><td>1101</td><td>3.50x</td><td></td><td>1.60</td><td></td><td>0.29</td></tr>
<tr><td>1110</td><td>3.75x</td><td></td><td>1.60</td><td></td><td>0.27</td></tr>
<tr><td>1111</td><td>4.00x</td><td>1.48</td><td>1.60</td><td>1.73</td><td>0.25</td></tr>
</table>
</td></tr>
</table>

6.2.5 Power Down Registers

- **Registers to Control Each Channel Reset**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x97	CH_RST_4	[3]	0xF	0x0F	**CH_RST_x** **:** Each Video Channel Reset (x = channel number) **0** : Channel_x Reset **1** : Channel_x On
		CH_RST_3	[2]			
		CH_RST_2	[1]			
		CH_RST_1	[0]			

- **Registers to Control CLK Power Down**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0x98	PD_DEC_4	[3]	0x00	0x00	**PD_DEC_x** **:** Each Decoder Clock Power Down (x = channel number) **0** : Decoder Clock Power On **1** : Decoder Clock Power Off
		PD_DEC_3	[2]			
		PD_DEC_2	[1]			
		PD_DEC_1	[0]			
	0x9A	AUD_RST	[4]	0x0	0x0	**AUD_RST** **:** Audio Reset **0** : Audio On **1** : Audio Reset
		PD_AUD	[0]	0x00	0x00	**PD_AUD** **:** Audio Clock Power Down

6.2.6 MPP Control Registers

- **Registers to Control MPP**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xB1	MPP1_DIR	[0]	0x00	0x00	**MPPx_DIR** **:** MPPx pin direction control (x = MPP pin number) **0** : Output Direction **1** : Input Direction
		MPP2_DIR	[1]			
		MPP3_DIR	[2]			
		MPP4_DIR	[3]			
	0xB2	MPP1_CLK	[0]	0x00	0x00	**MPPx_CLK** **:** MPPx Clock Enable (x = MPP pin number) **0** : MPP Signal out from MPPx_pin. **1** : Selected Clock among BANK1, 0xB4~BB Out from MPPx_pin
		MPP2_CLK	[1]			
		MPP3_CLK	[2]			
		MPP4_CLK	[7]			
	0xB3	MPP1_INV	[0]	0x00	0x00	**MPPx_INV** **:** MPPx pin output signal inversion (x = MPP pin number)
		MPP2_INV	[1]			
		MPP3_INV	[2]			
		MPP4_INV	[3]			

- **Registers to Control MPP**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xB4	MPP_CLK1_SEL	[7:4]	0x40	0x40	**MPP_CLKx_SEL** (x = MPP Pin number) **:** The Same as VCLKx Condition (VCLK = Bank1 0xCC~CF)
	0xB5	MPP_CLK2_SEL				
	0xB6	MPP_CLK3_SEL				
	0xB7	MPP_CLK4_SEL				
	0xB4	MPP_CLK1_DLY_SEL	[3:0]			**MPP_CLKx_DLY_SEL** (x = MPP Pin number) **:** The Same as VCLKx_DLY_SEL Condition (VCLKx_ DLY_SEL= Bank1 0xCC~CF)
	0xB5	MPP_CLK2_DLY_SEL				
	0xB6	MPP_CLK3_DLY_SEL				
	0xB7	MPP_CLK4_DLY_SEL				

6.2.7 Video Output Control Registers

- **Registers to Select Video Output**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xC0	VPORT1_SEQ1	[3:0]	0x00	0x00	**VPORTx_SEQy** **:** Select the type of output video signal through each video output port (x = VDO output port number, y= channel count for 1 port) **0** : Nomal Display of Channel 1 **1** : Nomal Display of Channel 2 **2** : Nomal Display of Channel 3 **3** : Nomal Display of Channel 4 **4** : Only Y Display of Channel 1 **5** : Only Y Display of Channel 2 **6** : Only Y Display of Channel 3 **7** : Only Y Display of Channel 4 **8** : H_Half Display of Channel 1 **9** : H_Half Display of Channel 2 **A** : H_Half Display of Channel 3 **B** : H_Half Display of Channel 4 **C** : Only C Display of Channel 1 **D** : Only C Display of Channel 2 **E** : Only C Display of Channel 3 **F** : Only C Display of Channel 4
		VPORT1_SEQ2	[7:4]			
	0xC1	VPORT1_SEQ3	[3:0]	0x00	0x00	
		VPORT1_SEQ4	[7:4]			
	0xC2	VPORT2_SEQ1	[3:0]	0x11	0x11	
		VPORT2_SEQ2	[7:4]			
	0xC3	VPORT2_SEQ3	[3:0]	0x11	0x11	
		VPORT2_SEQ4	[7:4]			
	0xC4	VPORT3_SEQ1	[3:0]	0x22	0x22	
		VPORT3_SEQ2	[7:4]			
	0xC5	VPORT3_SEQ3	[3:0]	0x22	0x22	
		VPORT3_SEQ4	[7:4]			
	0xC6	VPORT4_SEQ1	[3:0]	0x33	0x33	
		VPORT4_SEQ2	[7:4]			
	0xC7	VPORT4_SEQ3	[3:0]	0x33	0x33	
		VPORT4_SEQ4	[7:4]			

- **Registers to Select Video Output**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xC8	VPORT_1_CH_OUT_SEL	[7:4]	0x2	0x2	**VPORT_x_CH_OUT_SEL** **:** Select the output form of the data generated in case that the system is not set at No Video. (x = VDO output port number) **0** : 1-Port 1CH data **2** : 1-Port 2CH time-mixed data **8** : 1-Port 4CH time-mixed data **Etc.:** Don't use
	0xC9	VPORT_2_CH_OUT_SEL	[3:0]	0x2	0x2	

- **Registers to Control Video Output Port Enable**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xCA	VCLK_4_EN	[7]	0xF	0xF	**VCLK_x_EN** **:** Video Output Port_x CLK Enable (x = VDO output port number) **0** : Disable **1** : Enable
		VCLK_3_EN	[6]			
		VCLK_2_EN	[5]			
		VCLK_1_EN	[4]			
		VDO_4_EN	[3]	0xF	0xF	**VDO_x_EN** **:** Video Output Port_x VDO Enable (x = VDO output port number) **0** : Disable **1** : Enable
		VDO_3_EN	[2]			
		VDO_2_EN	[1]			
		VDO_1_EN	[0]			

- **Registers to Control Data**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xCB	OUT_DATA_4_INV	[3]	0	0	**VDO_INV_x** **:** It sorts output video data inversely. (**0 :** [7:0], **1 :** [0:7]) **OUT_DATA_1_INV :** VDO_1 Port output order control **OUT_DATA_2_INV :** VDO_2 Port output order control **OUT_DATA_3_INV :** VDO_3 Port output order control **OUT_DATA_4_INV :** VDO_4 Port output order control
		OUT_DATA_3_INV	[2]			
		OUT_DATA_2_INV	[1]			
		OUT_DATA_1_INV	[0]			

- **Registers to Select Video Output Clock**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
1	0xCC	VPORT_1_OCLK_SEL	[7:4]	0x46	0x46	**VPORT_x_OVCLK_SEL** **:** Select clock frequency and phase of each port. (x = Port number) **0~3 : PLL divided by 4** with phase#1~4 (74.25Mhz) **4~5 : PLL divided by 2** with phase#1~2 (148.5Mhz) **8~B : PLL divided by 8** with phase#1~4(37.125Mhz)
	0xCD	VPORT_2_OCLK_SEL				
	0xCE	VPORT_3_OCLK_SEL				
	0xCF	VPORT_4_OCLK_SEL				
	0xCC	VPORT_1_OCLK_DLY_SEL	[3:0]			**VPORT_x_OVCLK_DLY_SEL** **:** Delay the output clock in the unit of ≒ (VCLK / 16) ns. Can be delayed up (x = Port number) . **0 :** ≒ (VCLK / 16) *** 0** ns. **4 :** ≒ (VCLK / 16) *** 4** ns # Delay value = (VCLK / 16) ***** DLY_SEL Value ns
	0xCD	VPORT_2_OCLK_DLY_SEL				
	0xCE	VPORT_3_OCLK_DLY_SEL				
	0xCF	VPORT_4_OCLK_DLY_SEL				

6.2.8 MOTION Registers

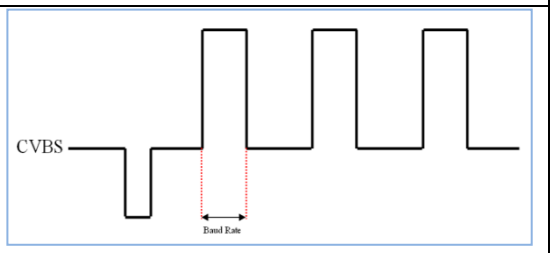
- **Registers to Detect Motion**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			FHD	HD	
2	0x00	CH1_MOTION_OFF	[0]	0xED	0x09	**CHx_MOTION_OFF** **:** Motion Detection On/Off Selection (x = channel number) **0 :** Motion detection on **1 :** Motion detection off
	0x07	CH2_MOTION_OFF				
	0x0E	CH3_MOTION_OFF				
	0x15	CH4_MOTION_OFF				

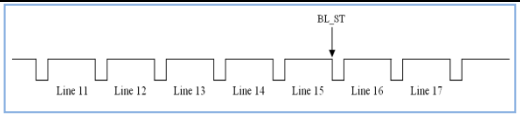
6.2.9 COAXIAL Registers

- CH1 Coaxial Register : Bank3 0x00~0x7F
- CH2 Coaxial Register : Bank3 0x80~0xFF
- CH3 Coaxial Register : Bank4 0x00~0x7F
- CH4 Coaxial Register : Bank4 0x80~0xFF

● **Registers to Control Baud Rate**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x00 / 0x80	CHx_BAUD	[7:0]	0x27	0x27	**CHx_BAUD** (x = Channel Number) **:** A-CP TX Baud Rate
	0x02 / 0x82	CHx_PELCO_BAUD	[7:0]	0x1B	0x1B	**CHx_PELCO_BAUD** (x = Channel Number) **:** PELCO TX Baud Rate
Coaxial protocol 1H Line						

● **Registers to Control Start Point of VBI(Vertical Blank Interval)**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x04 / 0x84	CHx_BL_TXST[15:8]	[7:0]	0x00	0x00	**CHx_BL_TXST** (x = Channel Number) **:** A-CP Protocol TX start Line in VBI
	0x03 / 0x83	CHx_BL_TXST[7:0]	[7:0]	0x0E	0x0E	
	0x05 / 0x85	CHx_ACT_LEN	[3:0]	0x03	0x03	**CHx_ACT_LEN** (x = Channel Number) **:** A-CP Line number
	0x08 / 0x88	CHx_PELCO_TXST [15:8]	[7:0]	0x00	0x00	**CHx_PELCO_TXST** (x = Channel Number) **:** PELCO Protocol TX Start Line in VBI
	0x07 / 0x87	CHx_PELCO_TXST [7:0]	[7:0]	0x0E	0x0E	
Coaxial protocol Active Start Point of VBI(Vertical Blank Interval)						

- **Registers to Control Coaxial Protocol**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x09 / 0x89	CHx_COAX_SW_RST	[4]	0x08	0x08	**CHx_COAX_SW_RST** (x = Channel Number) **:** Coaxial Software Reset
		CHx_CNT_MODE	[3]			**CHx_CNT_MODE** (x = Channel Number) **:** A-CP Protocol Enable Signal
		CHx_TX_START	[0]			**CHx_TX_START** (x = Channel Number) **:** A-CP Protocol Enable Signal
	0x0A / 0x8A	CHx_TX_BYTE_LENGTH	[4:0]	0x03	0x03	**CHx_TX_BYTE_LENGTH** (x = Channel Number) **:** Transmission amount In A-CP Protocol
	0x0B / 0x8B	CHx_PELCO_8BIT	[7]	0x10	0x10	**CHx_PELCO_8BIT** (x = Channel Number) **:** Pelco Protocol 8Bit mode Selection **0 :** Pelco Protocol Exp mode **1 :** Pelco Protocol 8bit mode
		CHx_LINE_8BIT	[4]			**CHx_LINE_8BIT** (x = Channel Number) **:** A-CP Protocol Origin Mode Selection **0 :** Pelco Protocol Mode **1 :** A-CP Protocol Origin Mode
		CHx_PACKET_MODE	[2:0]			**CHx_PACKET_MODE** (x = Channel Number) **:** Coaxial Protocol Type **2 :** Pelco Protocol Origin Mode **4 :** Pelco Protocol Exp mode(Pelco_32bit Mode) **Others :** Manual
	0x0C / 0x8C	CHx_PELCO_CTEN	[0]	0x00	0x00	**CHx_PELCO_CTEN** (x = Channel Number) **:** PELCO Protocol Enable Bit (Active High)
	0x0E / 0x8E	CHx_BL_HSP [15:7]	[7:0]	0x00	0x02	**CHx_BL_HSP** (x = Channel Number) **:** Start Point in Coaxial Protocol Active Line
	0x0D / 0x8D	CHx_BL_HSP [7:0]	[7:0]	0xB4	0x48	
	0x0F / 0x8F	CHx_PELCO_SHOT	[0]	0x00	0x00	**CHx_PELCO_SHOT** (x = Channel Number) **:** PELCO Protocol One Operation Enable signal

- **Registers to Control Coaxial Data**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x10 / 0x90	CHx_TX_DATA_01	[7:0]	0x00	0x00	**CHx_TX_DATA_01 ~ CHx_TX_DATA_04** (x = Channel Number) : 1st field Data in A-CP Protocol
	0x11 / 0x91	CHX_TX_DATA_02	[7:0]	0x10	0x10	
	0x12 / 0x92	CHX_TX_DATA_03	[7:0]	0x18	0x18	
	0x13 / 0x93	CHX_TX_DATA_04	[7:0]	0xFF	0xFF	
	0x14 / 0x94	CHX_TX_DATA_05	[7:0]	0xAA	0xAA	**CHx_TX_DATA_05 ~ CHx_TX_DATA_08** (x = Channel Number) : 2nd field Data in A-CP Protocol
	0x15 / 0x95	CHX_TX_DATA_06	[7:0]	0x3C	0x3C	
	0x16 / 0x96	CHX_TX_DATA_07	[7:0]	0xFF	0xFF	
	0x17 / 0x97	CHX_TX_DATA_08	[7:0]	0xFF	0xFF	
	0x18 / 0x98	CHX_TX_DATA_09	[7:0]	0xAA	0xAA	**CHx_TX_DATA_09 ~ CHx_TX_DATA_12** (x = Channel Number) : 3rd field Data in A-CP Protocol
	0x19 / 0x99	CHX_TX_DATA_10	[7:0]	0x1B	0x1B	
	0x1A / 0x9A	CHX_TX_DATA_11	[7:0]	0x00	0x00	
	0x1B / 0x9B	CHX_TX_DATA_12	[7:0]	0x00	0x00	
	0x1C / 0x9C	CHX_TX_DATA_13	[7:0]	0xAA	0xAA	**CHx_TX_DATA_13 ~ CHx_TX_DATA_16** (x = Channel Number) : 4th field Data in A-CP Protocol
	0x1D / 0x9D	CHX_TX_DATA_14	[7:0]	0x3B	0x3B	
	0x1E / 0x9E	CHX_TX_DATA_15	[7:0]	0x00	0x00	
	0x1F / 0x9F	CHX_TX_DATA_16	[7:0]	0x00	0x00	

- **Registers to Control Coaxial Data**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x20 / 0xA0	CHx_PELCO_TXDAT_01	[7:0]	0x00	0x00	**CHx_PELCO_TXDAT_01 ~ CHx_PELCO_TXDAT_02** : 18th Line in PELCO Protocol (x = Channel Number)
	0x21 / 0xA1	CHx_PELCO_TXDAT_02	[7:0]	0x00	0x00	
	0x22 / 0xA2	CHx_PELCO_TXDAT_03	[7:0]	0x00	0x00	**CHx_PELCO_TXDAT_03 ~ CHx_PELCO_TXDAT_04** : 19th Line in PELCO Protocol (x = Channel Number)
	0x23 / 0xA3	CHx_PELCO_TXDAT_04	[7:0]	0x00	0x00	

Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x2C / 0xAC	CHx_VSO_INV	[7:0]	0x00	0x00	**CHx_VSO_INV** (x = Channel Number) **:** Vertical Sync Inverter (Active High)
	0x2D / 0xAD	CHx_HSO_INV	[7:0]	0x00	0x00	**CHx_HSO_INV** (x = Channel Number) **:** Horizontal Sync Inverter (Active High)
	0x2F / 0xAF	CHx_EVEN_SUM	[7:0]	0x00	0x00	Control Protocol Active line on each field

Registers to Control Coaxial Protocol

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x3A / 0xBA	CHx_CLEAN	[0]	0x00	0x00	**CHx_CLEAN** (x = Channel Number) **:** RX Register is Read Only. So it need clean Condition First, this register set ON. Second, Read I2C Protocol 0x90. And then Clean RX Registers.

Registers to Read Coaxial Status

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x50 / 0xD0	CHx_PELCO_8_00	[7:0]	Read	Read	**CHx_PELCO_8_00 ~ CHx_PELCO_8_07** (x = Channel Number) **:** Coaxial Output 8bit Data Read Register
	0x51 / 0xD1	CHx_PELCO_8_01	[7:0]	Read	Read	
	0x52 / 0xD2	CHx_PELCO_8_02	[7:0]	Read	Read	
	0x53 / 0xD3	CHx_PELCO_8_03	[7:0]	Read	Read	
	0x54 / 0xD4	CHx_PELCO_8_04	[7:0]	Read	Read	
	0x55 / 0xD5	CHx_PELCO_8_05	[7:0]	Read	Read	
	0x56 / 0xD6	CHx_PELCO_8_06	[7:0]	Read	Read	
	0x57 / 0xD7	CHx_PELCO_8_07	[7:0]	Read	Read	

Registers to Read Coaxial Status

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x5C / 0xDC	CHx_RX_DONE	[0]	Read	Read	**CHx_RX_DONE** (x = Channel Number) : Coaxial RX Request Done

Registers to Read Coaxial Status

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x5D / 0xDD	CHx_RX_COAX_DUTY	[7:0]	Read	Read	**CHx_RX_COAX_DUTY** (x = Channel Number) **:** Coaxial RX 8bit DUTY Read

- **Registers to Control Coaxial Protocol**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x60 / 0xE0	CHx_ DEVICE_ID	[7:0]	0x84	0x84	**CHx_ DEVICE_ID** (x = Channel Number) : Define Device_ID in Protocol's Header
	0x62 / 0xE2	CHx_RX_AREA	[7:0]	0x06	0x06	**CHx_RX_AREA** (x = Channel Number) **:** Coaxial RX Area 8-bit
	0x63 / 0xE3	CHx_DELAY_ON	[4]	0x01	0x01	**CHx_DELAY_ON** (x = Channel Number) : Enable to use DELAY CNT Register
		CHx_COMM_ON	[0]			**CHx_COMM_ON** (x = Channel Number) **:** Coaxial RX Software Reset
	0x64 / 0xE4	CHx_DELAY_CNT	[7:0]	0x00	0x00	**CHx_DELAY_CNT** (x = Channel Number) : How many delay input signal based clock

- **Registers to Control Coaxial Protocol**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x65 / 0xE5	CHx_ MSB	[0]	0x01	0x01	**CHx_ MSB** (x = Channel Number) **:** Coaxial RX MSB Change Mode
	0x66 / 0xE6	CHx_A_DUTY_ON	[7]	0x80	0x80	**CHx_A_DUTY_ON** (x = Channel Number) **:** Coaxial RX DUTY Mode
	0x67 / 0xE7	CHx_INT_MODE	[0]	0x01	0x01	**CHx_INT_MODE** (x = Channel Number) **:** Coaxial RX Interrupt Mode
	0x68 / 0xE8	CHx_RX_SZ	[7:4]	0x50	0x50	**CHx_RX_SZ** (x = Channel Number) **:** Coaxial RX Line MAX Set
	0x69 / 0xE9	CH1_M_DUTY	[7:0]	0x00	0x00	**CH1_M_DUTY** (x = Channel Number) **:** Coaxial RX DUTY Set
	0x6A / 0xEA	CH1_RX_START_POSITION	[7:0]	0x00	0x00	**CH1_RX_START_POSITION** (x = Channel Number) **:** Coaxial RX Start Point in Line

- **Registers to Read Coaxial Status**

ADDRESS		REGISTER NAME	BITS	VALUE		DESCRIPTION
Bank	Addr			30P	25P	
3~4	0x6C / 0xEC	CHx_PELCO16_00 [7:0]	[7:0]	Read	Read	**CHx_PELCO16_00** (x = Channel Number) : Coaxial Output 16bit Data1 Read Register
	0x6D / 0xED	CHx_PELCO16_00 [15:8]	[7:0]	Read	Read	
	0x6E / 0xEE	CHx_PELCO16_01 [7:0]	[7:0]	Read	Read	**CHx_PELCO16_01** (x = Channel Number) : Coaxial Output 16bit Data2 Read Register
	0x6F / 0xEF	CHx_PELCO16_01 [15:8]	[7:0]	Read	Read	
	0x70 / 0xF0	CHx_PELCO16_02 [7:0]	[7:0]	Read	Read	**CHx_PELCO16_02** (x = Channel Number) : Coaxial Output 16bit Data2 Read Register
	0x71 / 0xF1	CHx_PELCO16_02 [15:8]	[7:0]	Read	Read	
	0x72 / 0xF2	CHx_PELCO16_03 [7:0]	[7:0]	Read	Read	**CHx_PELCO16_03** (x = Channel Number) : Coaxial Output 16bit Data2 Read Register
	0x73 / 0xF3	CHx_PELCO16_03 [15:8]	[7:0]	Read	Read	
	0x74 / 0xF4	CHx_PELCO16_04 [7:0]	[7:0]	Read	Read	**CHx_PELCO16_04** (x = Channel Number) : Coaxial Output 16bit Data2 Read Register
	0x75 / 0xF5	CHx_PELCO16_04 [15:8]	[7:0]	Read	Read	
	0x76 / 0xF6	CHx_PELCO16_05 [7:0]	[7:0]	Read	Read	**CHx_PELCO16_05** (x = Channel Number) : Coaxial Output 16bit Data2 Read Register
	0x77 / 0xF7	CHx_PELCO16_05 [15:8]	[7:0]	Read	Read	
	0x78 / 0xF8	CHx_PELCO16_06 [7:0]	[7:0]	Read	Read	**CHx_PELCO16_06** (x = Channel Number) : Coaxial Output 16bit Data2 Read Register
	0x79 / 0xF9	CHx_PELCO16_06 [15:8]	[7:0]	Read	Read	

* Registers of Bank 5 ~ Bank 10 are not for users.

In this regard, please refer to the Guide note.

Chapter 7
Guide Note

7.1 Video Format Setting Register

Mode		CH	SP_MD	SD_MD	HD_MD	ADC_CLK	PRE_CLK	DEC_CLK	VCLK
		1	0x85[3:0]	0x81[7:4]	0x81[3:0]	1x84[3:0]	1x8C[3:0]	1x8C[7:4]	A: 1xCC[7:4]
		2	0x86[3:0]	0x82[7:4]	0x82[3:0]	1x85[3:0]	1x8D[3:0]	1x8D[7:4]	B: 1xCD[7:4]
		3	0x87[3:0]	0x83[7:4]	0x83[3:0]	1x86[3:0]	1x8E[3:0]	1x8E[7:4]	C: 1xCE[7:4]
		4	0x88[3:0]	0x84[7:4]	0x84[3:0]	1x87[3:0]	1x8F[3:0]	1x8F[7:4]	D: 1xCF[7:4]
AHD	1080P_30		0	0	2	0~3	0~3	4~5	4~5
	1080P_25		0	0	3	0~3	0~3	4~5	4~5
	720P_60		0	0	4	0~3	0~3	4~5	4~5
	720P_50		0	0	5	0~3	0~3	4~5	4~5
	720P_30		0	0	A	8~B	8~B	4~5	4~5
	720P_25		0	0	B	8~B	8~B	4~5	4~5
	SD_NT		0	C	0	6~7	6~7	4~5	4~5
	SD_PAL		0	D	0	6~7	6~7	4~5	4~5

7.2 Each Format FSC Setting Register

Mode		CH	Register BANK9			
		1	0x50	0x51	0x52	0x53
		2	0x54	0x55	0x56	0x57
		3	0x58	0x59	0x5A	0x5B
		4	0x5C	0x5D	0x5E	0x5F
AHD	1080P_30		0x2C	0xF0	0xCA	0x52
	1080P_25		0xAB	0x7D	0xC3	0x52
	720P_60		0x2C	0xF9	0xC5	0x52
	720P_50		0x2C	0xE7	0xCF	0x52
	720P_30		0xED	0x00	0xE5	0x4E
	720P_25		0x45	0x08	0x10	0x4F
	SD_NT		0x1E	0x7C	0xF0	0x21
	SD_PAL		0xCB	0x8A	0x09	0x2A

7.3 When Auto Detection, Video Format Classifier

Resolution	Field rate	Read Register value (Bank5~8 0xF0)	MODE
SD, 480i	60i	0x00	SD_480i60
SD, 576i	50i	0x10	SD_576i50
AHD, 720p	30	0x20	AHD_720p30
	25	0x21	AHD_720p25
	60	0x22	AHD_720p60
	50	0x23	AHD_720p50
AHD, 1080p	30	0x30	AHD_1080p30
	25	0x31	AHD_1080p25

7.4 Coaxial Setting Register

AHD								
bank	**addr**	**description**	**1080p**		**720p**			
			30p	**25p**	**30p**	**25p**	**60p**	**50p**
5~8	0x7C	COAX_RX_SYNC/SRC SEL	0x11		0x11		0x01	
3~4	0x00/ 0x80	CHx_BAUD	0x27		0x15		0x1A	
	0x03/ 0x83	CHx_BL_TXST	0x0E	0x0D	0x0E	0x0D	0x0E	0x0D
	0x0D/ 0x8D	BL_HSP	0x48	0xB4	0x30	0x35	0x20	0x16
	0x0E/ 0x8E	BL_HSP	0x02	0x00	0x00		0x00	
	0x05/ 0x85	CHx_ACT_LEN	0x03		0x03		0x03	
	0x0A/ 0x8A	CHx_TX_BYTE_LENGTH	0x03		0x03		0x03	
	0x0B/ 0x8B	CHx_PELCO_8BIT	0x10		0x10		0x10	
	0x2F/ 0xAF	CHx_EVEN_SUM	0x00		0x00		0x00	

※ If you want to know about 3/4/5M RT format, please contact us(sales@nextchip.com).

Chapter 8
ELECTRICAL CHARACTERISTICS

8.1 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
1.2V Power Supply Voltage	VDD1A/ VDD1D	-0.5	-	1.8	V	
3.3V Power Supply Voltage	VDD3A/ VDD3D	-0.5	-	4.6	V	
Voltage for Digital Input pins	V_{DI}	-0.5	-	VDD3D+ 0.5	V	
Voltage for Analog Input pins	V_{AI}	-0.5	-	1.92	V	
Storage Temperature	T_S	-50	-	150	℃	
Junction Temperature	T_J	-40	-	125	℃	
Vapor phase soldering (15 Sec)	T_{VSOL}	-	-	220	℃	

* **Note** : This Device should be operated under recommended operating condition. Since, absolute maximum rating condition can either cause device reliability problem or damage the device sufficiently to cause immediate failure.

8.2 RECOMMENDED OPERATING CONDITION

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
1.2V Power Supply Voltage	VDD1A/ VDD1D	1.1	1.2	1.3	V	
3.3V Power Supply Voltage	VDD3A/ VDD3D	3.0	3.3	3.6	V	
Ambient operating temperature	V_A	0	-	70	℃	

8.3 DC CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	
Input High Voltage	V_{IH}	2	-	VDD3D+0.3	V	
Input Leakage Current	I_L	-	-	±10	uA	
Input Capacitance	C_{IN}	-	5	-	pF	
Output Low Voltage	V_{OL}	-	-	0.4	V	
Output High Voltage	V_{OH}	2.4	-	-	V	
Tri-State Output Leakage Current	I_{OZ}	-	-	±10	uA	
Output Capacitance	C_{OUT}	-	5	-	pF	

8.4 AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	REMARKS
(Power Supply Current)						
1.2V Digital Power Supply Current	I_{VDD1D}	-	TBD	-	mA	
3.3V Digital Power Supply Current	I_{VDD3D}	-	TBD	-	mA	
1.2V Analog Power Supply Current	I_{VDD1A}		TBD		mA	
3.3V Analog Power Supply Current	I_{VDD3A}	-	TBD	-	mA	
(Clock Pin)						
SYS_CLK frequency	f_{SYS_CLK}	-	27.0	-	MHz	
SYS_CLK duty cycle	f_{DUTY}	45	-	55	%	
(Reset Pin)						
RSTB setup time	t_{SU}	1			uSec	
RSTB pulse width low	t_{PWL_rstb}	1			uSec	
RSTB release time (low to high)	t_{REL_rstb}	10			uSec	
(Host Interface Pins)						
SCL clock frequency	f_{SCL}	-	100	400	kHz	
Hold time(repeated) START condition.	$t_{HD:STA}$	0.6	-	-	uSec	
LOW period of the SCL clock	t_{LOW}	1.3	-	-	uSec	
HIGH period of the SCL clock	t_{HIGH}	0.6	-	-	uSec	
Set-up time for a repeated START condition	$t_{SU:STA}$	0.6	-	-	uSec	
Data hold time	t_{HD_DAT}	0	-	0.9	uSec	
Data set-up time	t_{SU_DAT}	100	-	-	ns	
Rise time of both SDA and SCL signals	t_r	20	-	300	ns	
Fall time of both SDA and SCL signals	t_f	20	-	300	ns	
Set-up time for STOP condition	$t_{SU:STO}$	0.6	-	-	uSec	
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	-	uSec	
Capacitive load for each bus line	C_b	-	-	400	pF	

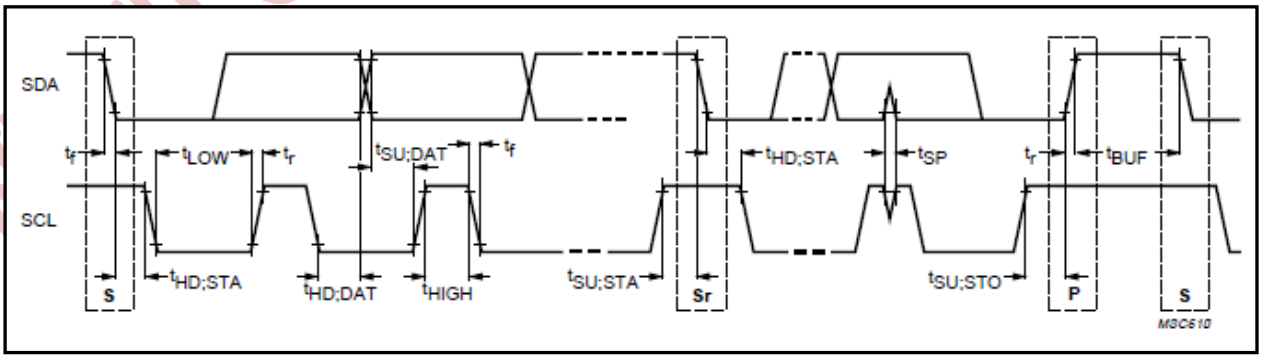


Figure 8.1 SCL and SDA Timing Diagram

Chapter 9
AUDIO SYSTEM APPLICATIONS

9.1 AUDIO 4-Channel Mode

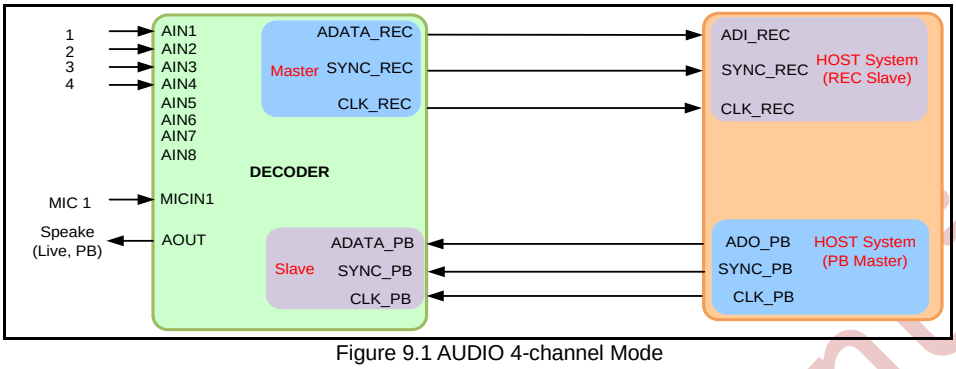


Figure 9.1 AUDIO 4-channel Mode

9.2 AUDIO 8-Channel Mode

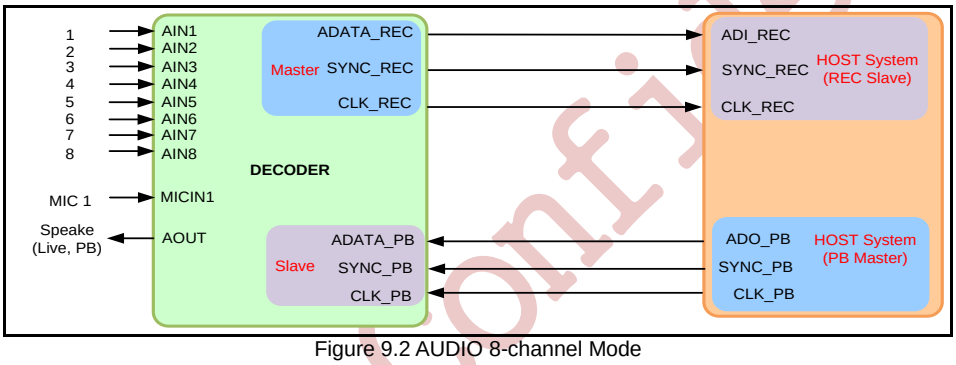


Figure 9.2 AUDIO 8-channel Mode

9.3 AUDIO 16-Channel Mode

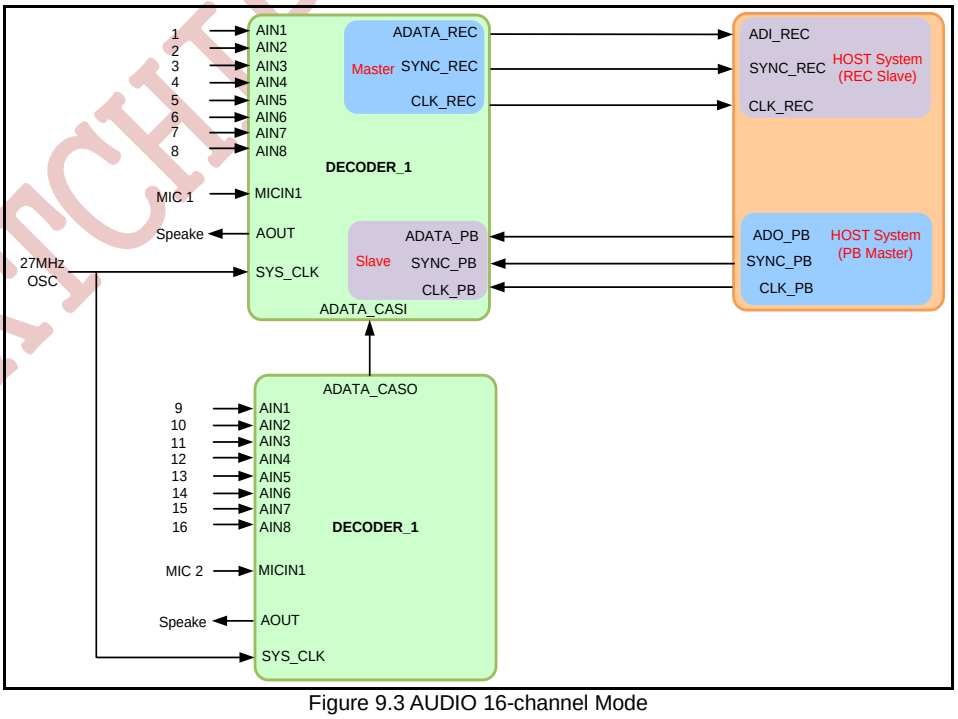


Figure 9.3 AUDIO 16-channel Mode

Chapter 10
PACKAGE INFORMATION

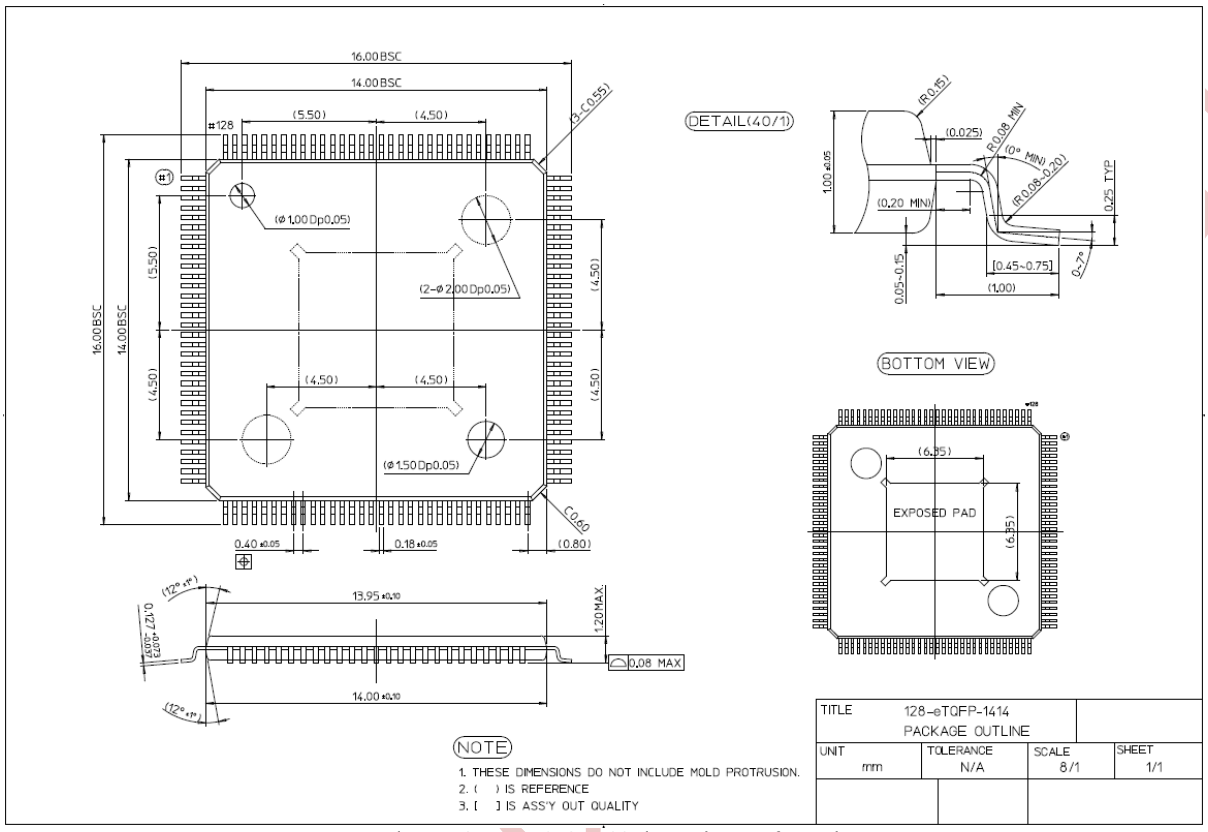


Figure 10.1 NVP6134 128Pin Package Information