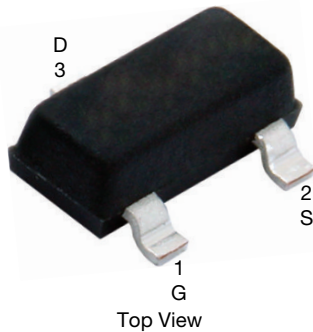


N-Channel 60 V (D-S) MOSFET

SOT-23 (TO-236)

Marking code: 7K

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	2
Q_g typ. (nC)	0.4
I_D (A)	0.3
Configuration	Single

FEATURES

- Low on-resistance: 2Ω
- Low threshold: 2 V (typ.)
- Low input capacitance: 25 pF
- Fast switching speed: 25 ns
- Low input and output leakage
- TrenchFET® power MOSFET
- 2000 V ESD protection
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


Note

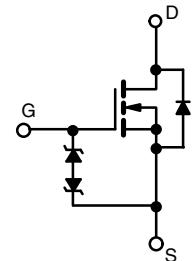
* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

BENEFITS

- Low offset voltage
- Low voltage operation
- Easily driven without buffer
- High speed circuits
- Low error voltage

APPLICATIONS

- Direct logic-level interface: TTL/CMOS
- Drivers: relays, solenoids, lamps, hammers, display, memories, transistors, etc.
- Battery operated systems
- Solid state relays



N-Channel MOSFET

ORDERING INFORMATION	
Package	SOT-23
Lead (Pb)-free	2N7002K-T1-E3
Lead (Pb)-free and halogen-free	2N7002K-T1-GE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150 \text{ }^\circ\text{C}$) ^b	I_D	$T_A = 25 \text{ }^\circ\text{C}$	0.3
		$T_A = 100 \text{ }^\circ\text{C}$	0.19
Pulsed drain current ^a	I_{DM}	0.8	A
Power dissipation ^b	P_D	$T_A = 25 \text{ }^\circ\text{C}$	0.35
		$T_A = 100 \text{ }^\circ\text{C}$	0.14
Maximum junction-to-ambient ^b	R_{thJA}	350	$^\circ\text{C/W}$
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Notes

- Pulse width limited by maximum junction temperature
- Surface mounted on FR4 board

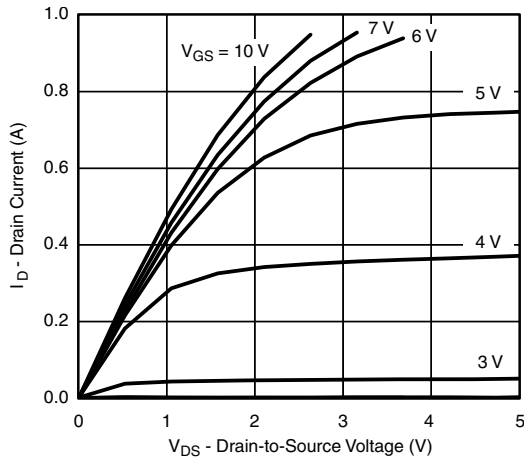
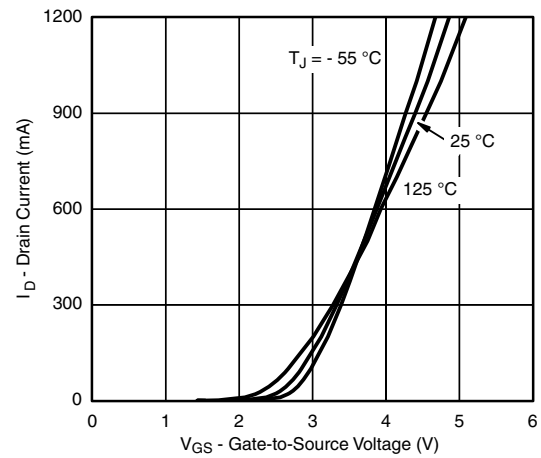
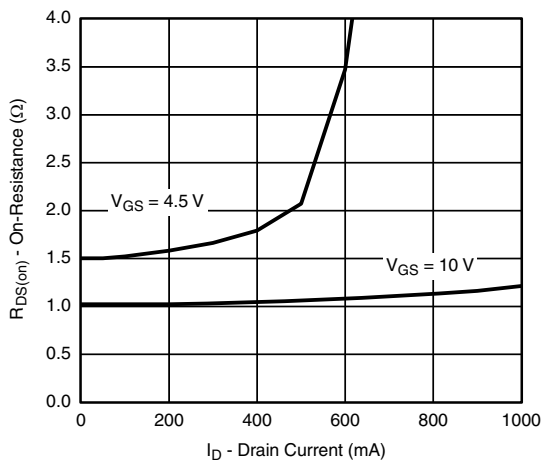
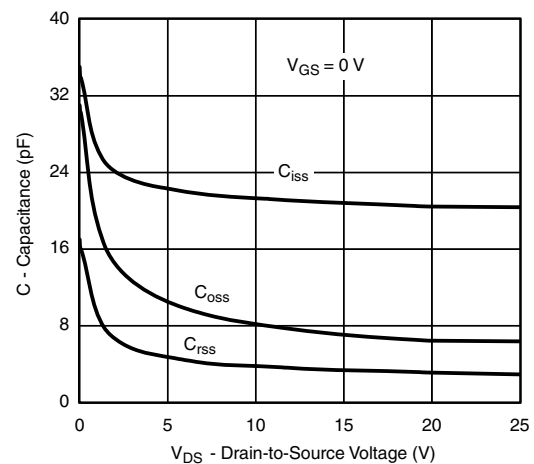
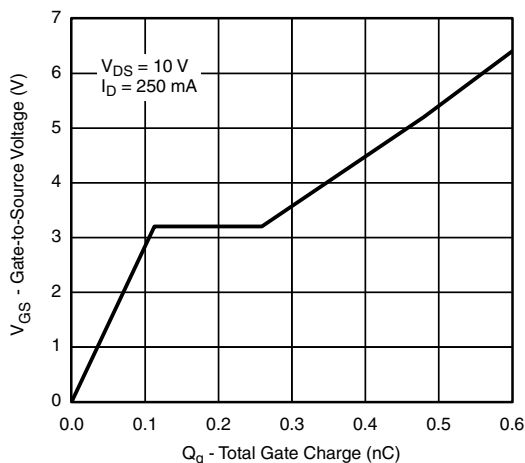
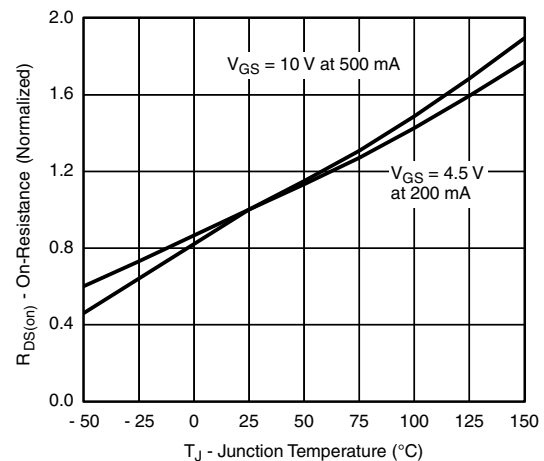


SPECIFICATIONS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP. ^a	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 10\text{ }\mu\text{A}$	60	-	-	V
Gate-threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	-	2.5	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	-	-	± 10	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 15\text{ V}$	-	-	1	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$	-	-	± 150	μA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}, T_J = 85\text{ }^\circ\text{C}$	-	-	± 1000	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 5\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	500	μA
On-state drain current ^b	$I_{D(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 7.5\text{ V}$	800	-	-	mA
		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}$	500	-	-	mA
Drain-source on-resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 500\text{ mA}$	-	-	2	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 200\text{ mA}$	-	-	4	Ω
Forward transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 200\text{ mA}$	100	-	-	mS
Diode forward voltage	V_{SD}	$I_S = 200\text{ mA}, V_{GS} = 0\text{ V}$	-	-	1.3	V
Dynamic ^{a, b}						
Total gate charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}$ $I_D \cong 250\text{ mA}$	-	0.4	0.6	nC
Input capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$	-	30	-	pF
Output capacitance	C_{oss}		-	6	-	
Reverse transfer capacitance	C_{rss}		-	2.5	-	
Switching ^{a, c}						
Turn-on time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 150\text{ }\Omega$ $I_D \cong 200\text{ mA}, V_{GEN} = 10\text{ V}, R_g = 10\text{ }\Omega$	-	-	25	ns
Turn-off time	$t_{d(off)}$		-	-	35	

Notes

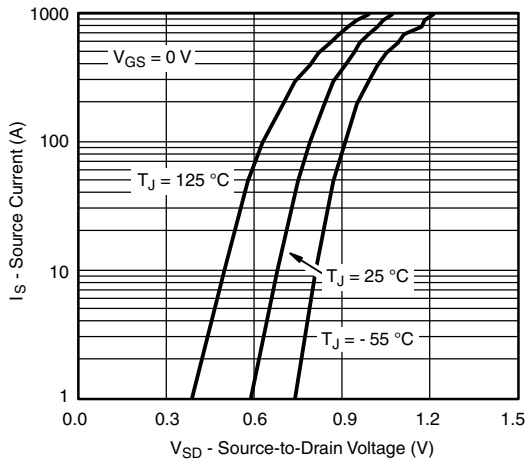
- a. For DESIGN AID ONLY, not subject to production testing
b. Pulse test: pulse width $\leq 300\text{ }\mu\text{s}$ duty cycle $\leq 2\%$
c. Switching time is essentially independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

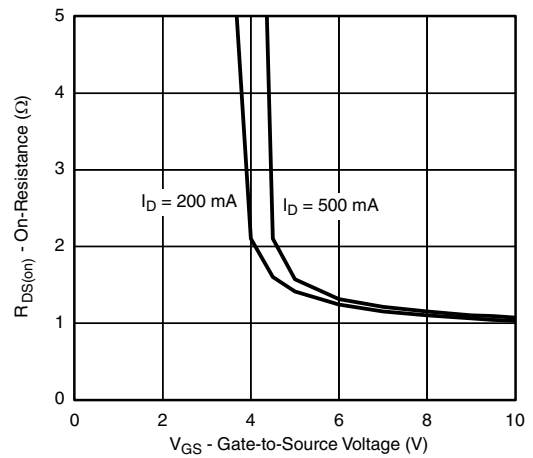
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current

Capacitance

Gate Charge

On-Resistance vs. Junction Temperature



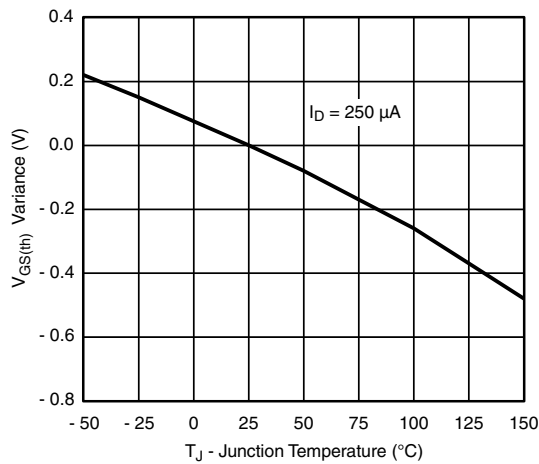
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



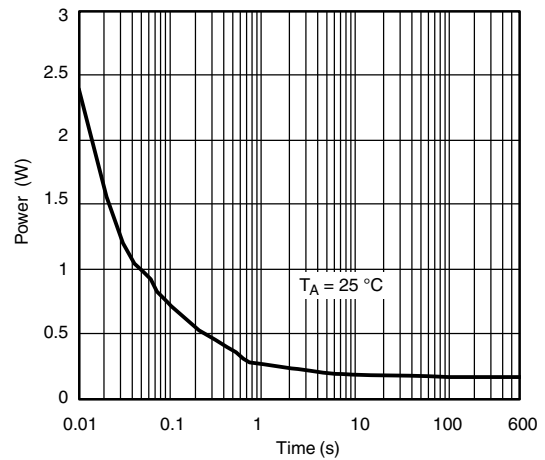
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-Source Voltage



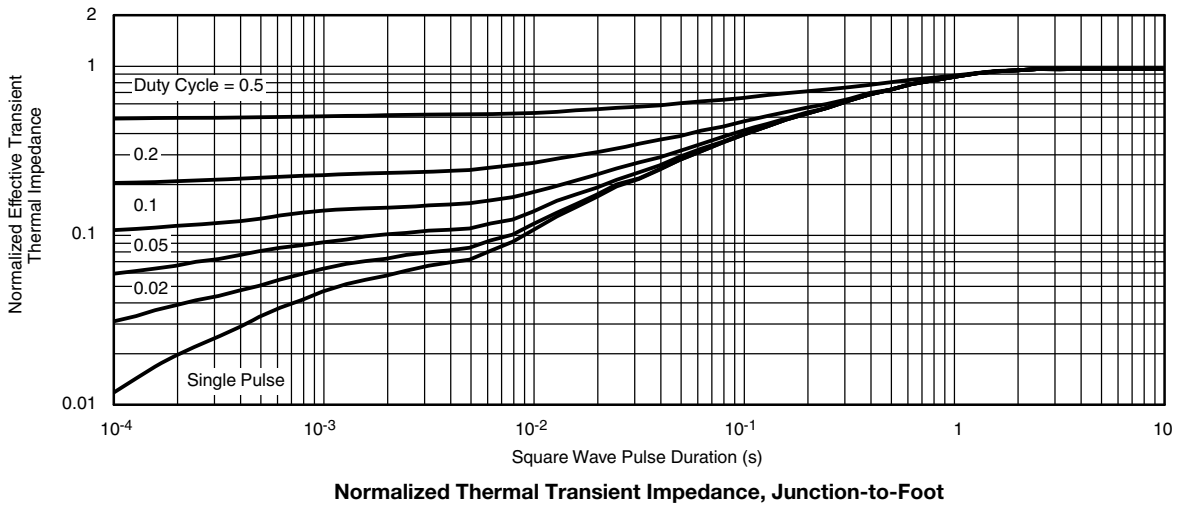
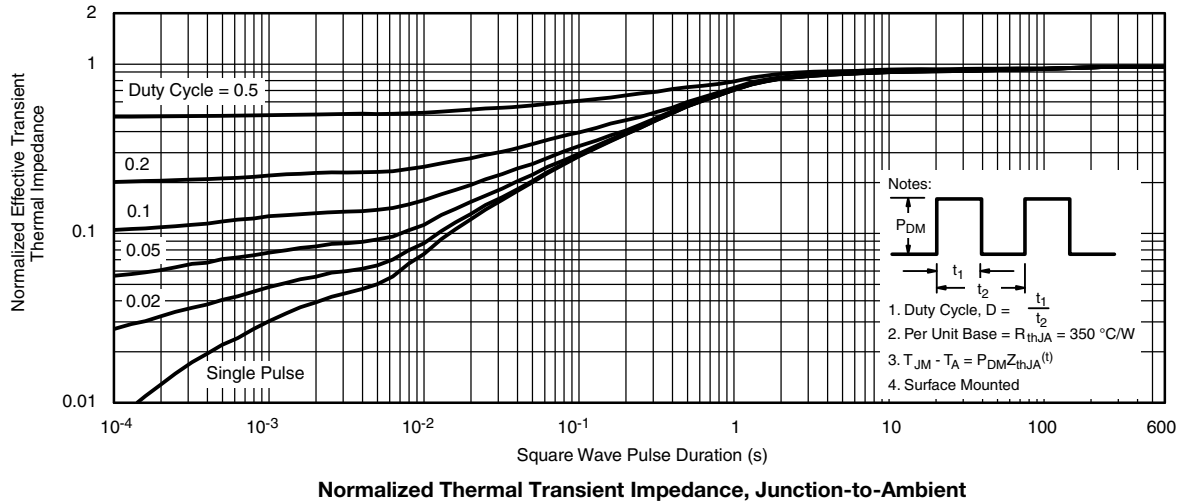
Threshold Voltage Variance Over Temperature



Single Pulse Power, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71333.

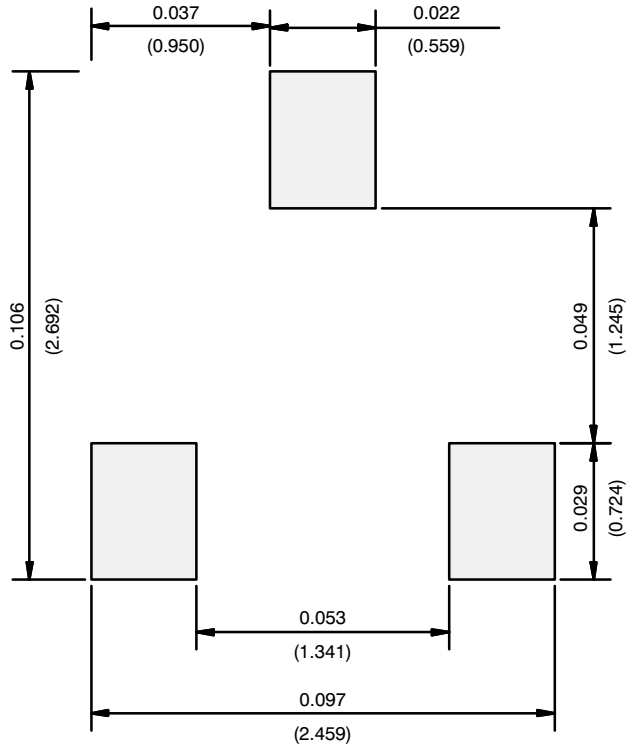
SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A ₁	0.01	0.10	0.0004	0.004
A ₂	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E ₁	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e ₁	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L ₁	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°

ECN: S-03946-Rev. K, 09-Jul-01
 DWG: 5479

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

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