HITACHI

SH7718/08/02 (SH-3 Series)

SuperH™ RISC Processor

Product Brief

Description

The SH7718/SH7708/SH7702 (SH-3 Series) are high performance, cost-effective, and highly integrated 32-bit RISC microprocessors for embedded applications. The SuperH™ architecture is the leader in code density among RISC microprocessors, reducing memory costs in embedded applications.

The SH-3 Series processors are used in consumer, data processing, industrial, and communication markets. Applications include handheld PCs, digital cameras, Internet appliances, security systems, hard disk drives, cellular phones, and protocol converters. The devices can be paired with a user-defined ASIC device to design a low cost, low IC count, and differentiated system.
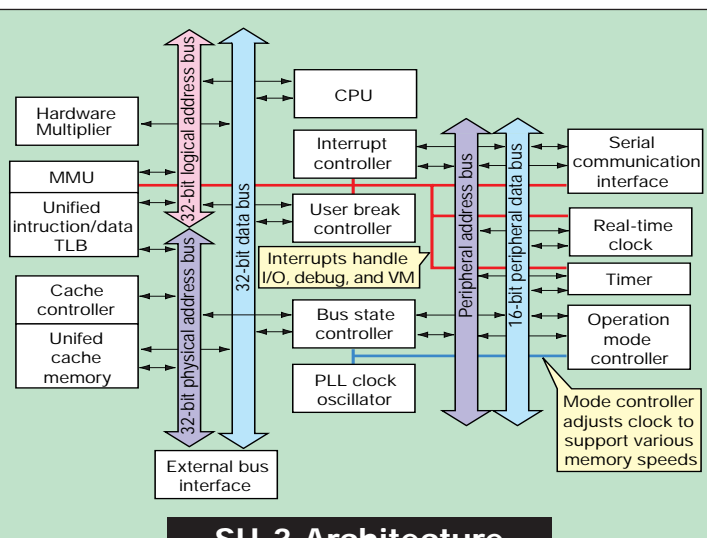
Hitachi optimized the SH7718/SH7708 MMU, cache size, and peripheral mix for Windows®CE applications. The SH7702 offers a reduced cache and package size for cost effective applications and other operating systems.

Hitachi SH-3 32-bit RISC Processor

Features

- General
  - 100 MHz/100 MIPS at 3.3 volts: SH7718/SH7708
  - 60 MHz/60 MIPS at 3.3 volts: SH7708
  - 45 MHz/45 MIPS at 3.3 volts: SH7702
  - 144 pin QFP (SH7718)
  - 144 pin TQFP (SH7708)
  - 120 pin TQFP (SH7702)

- CPU
  - Code compatible with SH7000/7600 series
  - 16 x 32-bit general purpose registers
  - 16-bit fixed instruction length for high code density
  - 32 x 32 --> 64 bits multiply-accumulate unit for special functions such as software modems
  - MMU Designed for Windows®CE 1KB, and 4KB page sizes, 128-entry, 4-way set associative TLB (SH7718/SH7708 only)
  - 5 stage pipeline

- FPU (SH7718 only)
  - Single precision
  - Single cycle FMAC
  - 200 MFLOPS

- Instruction set: 68 basic instruction types

- Memory
  - On-chip cache, unified instruction and data
    - 8KB: SH7718/SH7708
    - 2KB: SH7702
    - Write back or write through, LRU cache
    - Low voltage cache to reduce power consumption
  - On-chip bus state controller allows direct connection to DRAM, SDRAM, SRAM, ROM, and Flash ROM
    - 8, 16, or 32-bit data bus support (SH7718/SH7708)
    - 8 and 16-bit data bus support (SH7702)

SH-3 Architecture

- **Peripherals**
  - Timers, 3chx32-bits
  - Watchdog timer
  - Realtime clock
  - PCMCIA control logic
  - Serial communications interface, 1ch (asynchronous/synchronous, with smart card interface)
  - PLL with x1, x2, (x3 SH7718/SH7708 100 MHz only), x4, external clock capability
    - Interrupt controller

- General purpose I/O, 8 lines (SH7708-60 only)

- **Dynamic power control**
  - Low power modes: sleep and standby
  - Peripheral turn off capability
  - User break controller for on-chip debugging

Support

- **Hardware:**
  - Hitachi E7000 emulator and POD
  - Hitachi low cost evaluation board
  - Hitachi D9000 development platform for SH7708 and Windows®CE
  - Third party emulators - Hewlett-Packard, Orion

- **Software:**
  - Hitachi:
    - C, C++ compiler, assembler, simulator/debugger
  - Third parties:
    - C, C++ compiler, assembler, simulator/debugger, Cygnus Support (gnu), Green Hills Software, Microsoft® VC++ for Windows CE
    - Task and timing simulation - CARDtools™ Systems

- **Operating Systems:**
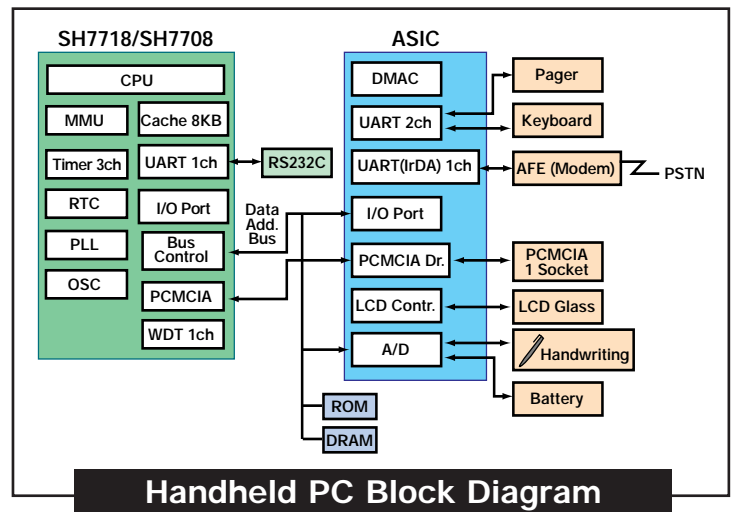 Geoworks, Hitachi OS, Java, LINUX, Nucleus+, OS-9, pSOS, VxWorks, Windows®CE

Middleware

- V.34 (up to 56 Kbps) Data/FAX software modem
- Voice recognition
- Voice compression
- Handwriting recognition
- JPEG video compression
- Image compression for FAX: MH, MR, MMR

Ordering Information

Part numbers:
SH7718R-HD6417718F100 (100 MHz, QFP)
SH7708R-HD6417708RF100 (100 MHz, QFP-144)
SH7708S-HD6417708SF60 (60 MHz, QFP-144)
SH7708S-HD6417708SX60 (60 MHz, TQFP-144)
SH7702-HD6417702X45 (45 MHz, TQFP-120)

Handheld PC Block Diagram

Complete SH-3 technical documentation is online at:
http://www.hitachi.com/semiconductor

This document may, wholly or partially, be subject to change without notice.

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